

ITS3: the ALICE Inner Tracking System upgrade

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The ALICE experiment at CERN is developing an upgrade to its vertexing detector in order to improve the impact parameter resolution at low transverse momenta, with a target timeline for installation during the third long shutdown of the LHC (2026–28). The concept consists in replacing the three innermost layers with wafer-scale monolithic active pixel sensors bent into truly cylindrical sensors wrapped around the beam pipe. The dramatic reduction in material budget (0.35% X_0 to 0.07% X_0 per layer), together with a thinner beam pipe (18 to 16.5 mm in radius) and a first layer closer to the interaction point (23 to 19 mm), are key features to increase the pointing resolution by at least a factor of 2 over all momenta.[1] This contribution provides an overview on the plans, challenges and status of the design and validation of the first wafer-scale silicon detector for high energy physics.

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1. Motivation and concept

The ALICE experiment at CERN is developing an upgrade of its vertexing detector in order to improve the impact parameter resolution at low transverse momenta. The one currently installed and operational goes under the name of Inner Tracking System 2 (ITS2, Figure 1a), as it is in turn an upgrade to the original ITS and was installed during the third long shutdown of the LHC (LS3) in 2021.

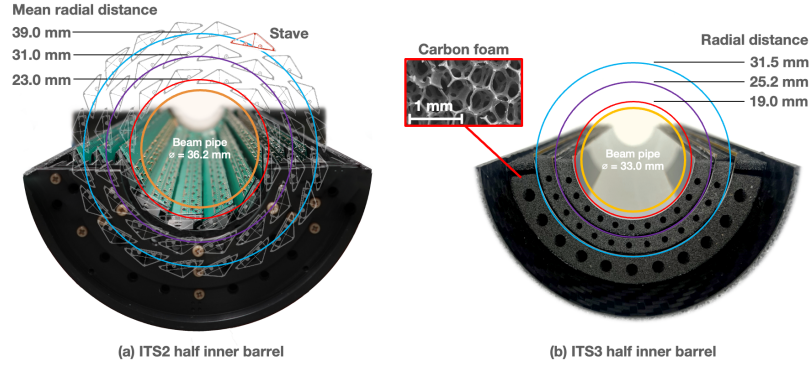


Figure 1: the ITS3 upgrade concept. Figure (a): the three innermost layers of ITS2 consist of 48 staves measuring 270 mm in length. Figure (b): the layers of the half barrels of ITS3 measure 266 mm in length and 58.7, 78.3, and 97.8 mm in width from innermost to outermost.

The ITS2 is a state-of-the-art detector. It is the largest monolithic active pixel sensors (MAPS) detector ever built, consisting of seven layers for a total area of 10 m^2 of MAPS and 12.5×10^9 pixels. Yet, room for improvement can be found by examining the material budget distribution of its innermost layer as a function of the azimuthal angle, shown in Figure 2.

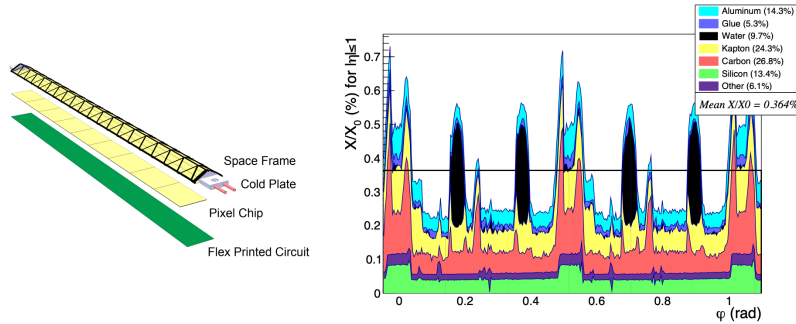


Figure 2: (left) components of an ITS2 stave and (right) material budget distribution of the ITS2 innermost layer as a function of the azimuthal angle.[1, 2]

The picture highlights two main opportunities for optimization. The first one is given by the fact that although lightweight, the detector is very dense, and the actual silicon is only 13.4% of the total material. Secondly, there are noticeable irregularities in the distribution, mainly due to the support and cooling structure, and the partial overlap between adjacent staves. These observations naturally define three main design goals for the new detector: switching to air cooling to remove the water cooling infrastructure; integrating power and data transmission on chip to remove the supply and readout circuit boards; adopting a self-supporting structure for the sensors, like arched silicon.

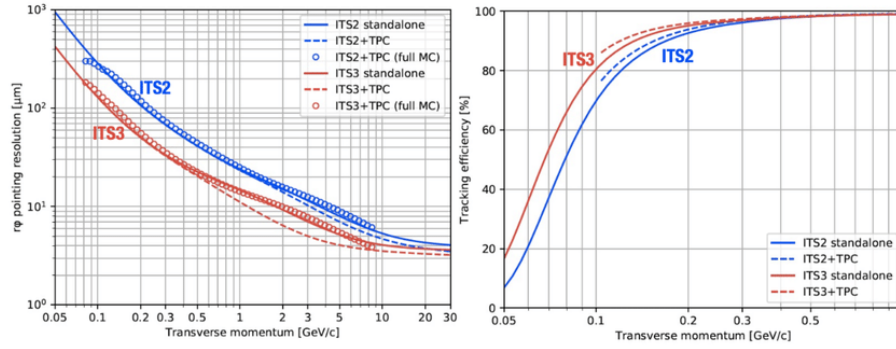


Figure 3: improvement in pointing resolution (left) and standalone tracking efficiency (right) as a function of the transverse momentum projected to be achieved by ITS3 (red) compared to ITS2 (blue).[1]

The resulting concept for the ITS3 upgrade is shown in Figure 1b. Full tracker half-layers will be covered by single wafer-scale CMOS MAPS bent detectors measuring up to $97.8 \times 266 \text{ mm}^2$ in size, manufactured in a commercial 65 nm technology developed by Tower Partners Semiconductor Co. (TPSCo).[8] Mechanical support is provided by carbon foam spacers. The three layers will be installed at a distance of 31.5, 25.2, and 19.0 mm from the interaction point, respectively — also requiring a thinner beam pipe. The material budget in the region close to the interaction point will be reduced from the current 0.35% X_0 down to 0.07% X_0 per layer in the region close to the interaction point. The improvement reached by ITS3 is reported in Figure 3; an increase of a factor of 2 is expected for the pointing resolution for the whole transverse momentum range.[2]

2. Sensor R&D

The target specifications for the ITS3 sensor are summarized in Table 1. In order to meet the requirements, three key innovations are being introduced and tested in the R&D phase for the first time in high energy physics, outlined in the following sections.

2.1 TPSCo 65 nm

Crucially, the TPSCo 65 nm technology can be produced on 300 mm wafers. This provides the sheer real estate needed to produce sensors in the size needed by ITS3. A smaller features also enables the design of detectors with more functionality and higher integration density, while at the same time lowering the material budget.

A first submission in TPSCo 65 nm named Multi-Layer Reticle 1 (MLR1) was received in summer 2021 and focused on a large number of small prototype structures in different processing flavors as a test of the technology. These test structures underwent a campaign of thorough verification both in terms of radiation hardness and pixel performance for high-energy physics applications.[4]

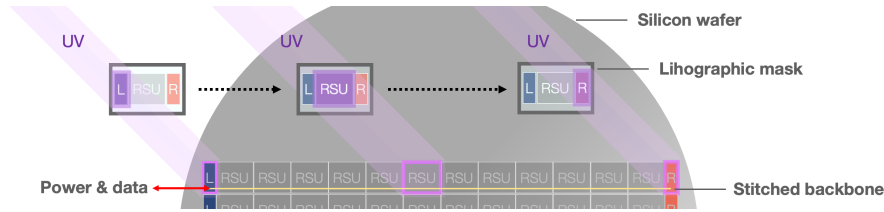
2.2 Stitching

In order to build detector elements larger than the reticle size, a process called stitching is used to join detector elements to build sensors up to 266 mm in length on a single wafer. All MAPS

	Layer 0	Layer 1	Layer 2
Radial position (mm)	19.0	25.2	31.5
Length (sensitive area) (mm)	260	260	260
Pseudo-rapidity coverage (w/r/t $z = 0$)	± 2.5	± 2.3	± 2.0
Active area (cm ²)	305	407	507
Pixel sensors dimensions (mm ²)	266×58.7	266×78.3	266×97.8
Number of sensors per layer	2		
Material budget ($\%X_0$ / layer)	0.07		
Silicon thickness (μm / layer)	≤ 50		
Power density (mW/cm ²)	40		
NIEL (1 MeV n_{eq} cm ⁻²)	10^{13}		
TID (kGray)	10		

Table 1: specifications and requirements for the Inner Tracking System 3.[1]

used in HEP, including the ALPIDE used in ITS2, have so far been limited in size by the typical field of view of the lithographic masks used in the fabrication process, that is about 3×2 cm². To cover larger surfaces, chips are mounted one next to each other as tiles and read out independently by dedicated circuit boards. The additional structural support and electronics, however, negatively impacts the material budget.

**Figure 4:** schematic representation of the production of a wafer-scale stitched sensor.

The fabrication of a stitched sensor, shown in Figure 4, uses the conventional UV photolithographic process also used to manufacture conventional MAPS. The design of the chip is structured in subunits that exist on the reticle as independent blocks and include metal traces that allow for power and data transmission from side to side, called *backbone*. Transferring the units on the silicon wafer over adjacent locations with accurate translation and alignment ensures continuity between adjacent units at the boundaries. This provides the interconnection of the power and data lines needed to operate the stitched sensor as a single entity.

2.3 Thinning and bending

Lastly, the wafer is mechanically thinned down to approximately 50 μm . At this thickness, silicon becomes flexible and enables the self-supporting curved design on which the ITS3 concept is based [9]. The electro-mechanical integration of the bent sensor is dedicated a significant portion of the R&D effort. Special care must be taken to master the technique to bend the silicon, as well

as its integration in carbon foam with the appropriate properties, the forced air cooling and the interconnection with the external supply and readout infrastructure.[5]

3. ER1: the first monolithic stitched sensors for high energy physics

As part of the R&D milestones, MLR1 was followed by the Engineering Run 1 (ER1) submission. Completed in autumn 2022 and received in April 2023, it included two large stitched detector prototypes named Monolithic Stitched Sensor (MOSS) and Monolithic Stitched sensor with Timing (MOST).

MOSS was designed to validate manufacturing yield and feasibility of power and signal transmission over a length of 26 cm. It is a 6.7 megapixels sensor, measuring $1.4 \times 25.9 \text{ cm}^2$. As shown in figure 5, each of its ten subunits is composed of two half-units (*top* and *bottom*, that are also the power segmentation domains) with different pixel designs. The data can be read out either locally from a single half-unit or from the left endcap thanks to the stitched backbone.

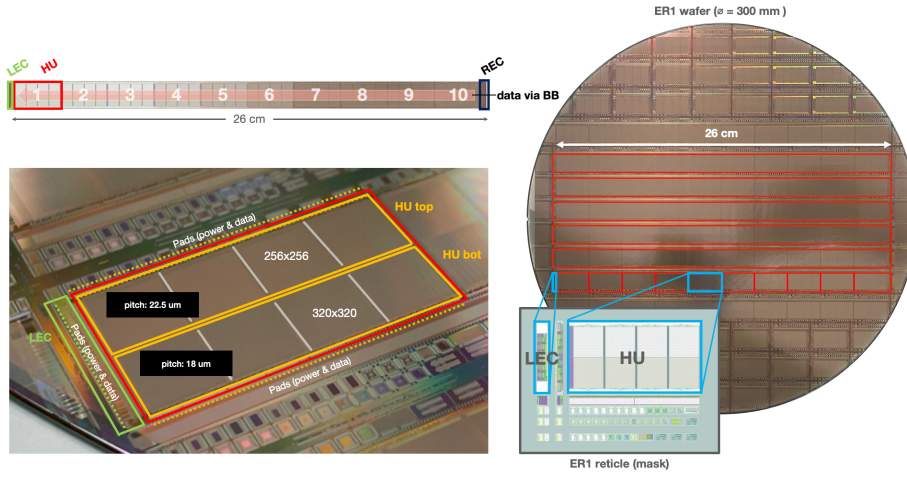


Figure 5: ER1 wafer and design reticle, and the MOSS stitched design.

The MOST, shown in Figure 6, measures $0.25 \times 25.5 \text{ cm}^2$ and its design features an event-driven asynchronous readout with time-stamping, which allows for measurements of time of arrival and time over threshold. Its design is structured as independent groups of four pixels organized in 64 columns, which reduces the number of pixels or the size of the sectors that need to be powered down in case of defects. The dead-area is also reduced as the readout is distributed in the active matrix area, and it is more power efficient at low hit rates, as it requires no strobing or clock distribution. However, drawbacks include the need of off-chip decoding at data rates up to 2 Gbit/s and data packet collision at high hit rates due to the asynchronous sharing of transmission lines.

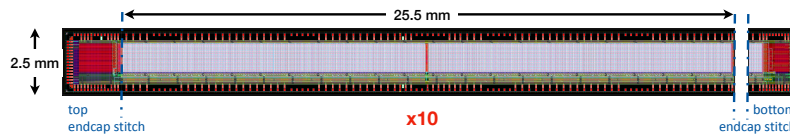


Figure 6: MOST structure. Only one of the ten subunits is shown here.

3.1 MOSS testing

A custom readout system has been developed to test the MOSS in all of its features and evaluate its functional yield at half unit, block, column/row/pixel level granularity. This was a challenge in itself, considering that more than 2000 connections are needed to operate it and the expertise required to handle, bond, and mechanically support such a huge and delicate sensor in a variety of use cases such as lab testing or test beams.

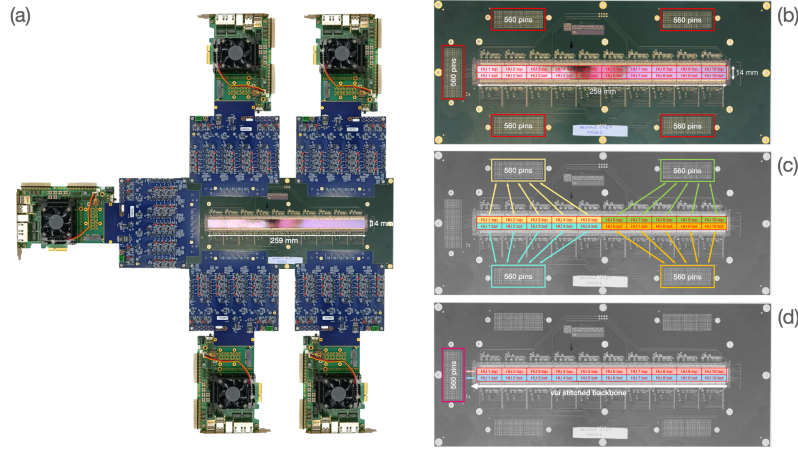


Figure 7: MOSS test system, with more than 2000 connections to operate the sensor from both its long and short edge.

The concept is shown in Figure 7 and it is based on three different types of boards. A *carrier card* is used to host and connect the MOSS chip as shown in figure 7. Five 560-pin connectors are located along the perimeter, four connectors dedicated to the chip's four quadrants, and a fifth to operate the chip via the stitched backbone. Five *proximity cards* provide additional powering and monitoring features, one for each quadrant and one for the top and bottom halves via the stitched backbone. Five *automation and readout modules* steer the proximity boards and interface the sensor control and readout with a computer.

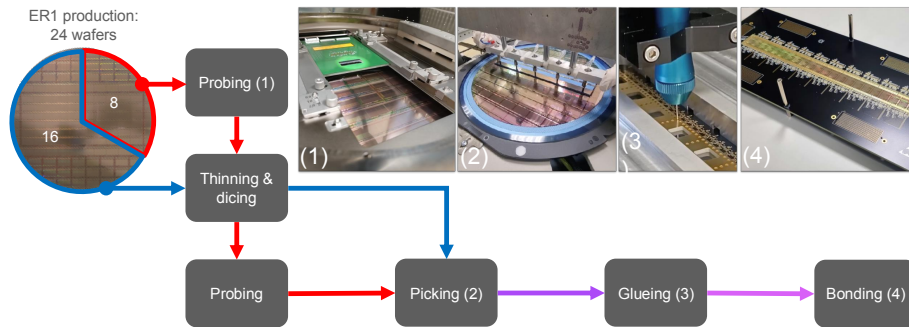


Figure 8: testing flow of the Engineering Run 1 production.

As shown in Figure 8, the ER1 production was in part wafer probed and then bonded on carrier, and in part directly bonded to be characterized in the laboratory. The wafer probing was carried out with a custom probe card. The picking, gluing and bonding tools were also custom developed by the collaboration. The MOSS is currently undergoing an extensive characterization campaign.

3.2 The final ITS3 sensor design

Two additional submissions labeled Engineering Run 2 (ER2) and Engineering Run 3 (ER3) are in the planning stage and their completion is expected in the second half of 2024 and 2025, respectively, and will include full-scale sensors as prototypes for the final system. Figure 9 shows the preliminary floorplan of the final stitched design. As shown in Figure 4, a Repeated Sensor Unit (RSU) is lithographed over the surface of the wafer and in a 12×5 grid. By stitching the RSUs along in rows of 12 units, a sensor segment named MONolithic Stitched Active pIXel (MOSAIX) is obtained, that can be powered and operated via its left endcap. The three layers for each half barrel are obtained by thinning and dicing the wafer and bending the resulting sensors. The specifications of the design were not yet final at the time of this contribution. ER2 and ER3 will be functionally equivalent, with the former being a pilot run of 48 wafers with the purpose of characterizing the design and the latter being the final production run.

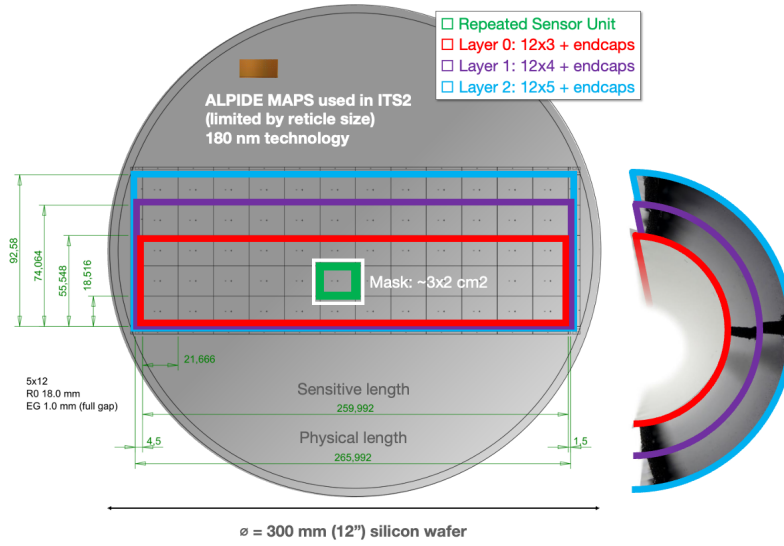


Figure 9: floorplan of the final sensor production.[1]

4. Summary and outlook

The ALICE experiment is developing an upgrade of its inner tracker based on wafer-scale truly cylindrical bent sensors. The breakthrough concept is enabled by the introduction for the first time in high energy physics of three key innovations, that is the 65 nm commercial technology by TPSCo, the stitching technique used to produce sensor larger than the usual lithographic mask, and the thinning and bending of the silicon wafer to achieve the curved geometry.

The R&D project already achieved the first major milestones, with the validation of the TPSCo 65 nm technology and the production and test of the first monolithic stitched sensors for high energy physics. The design of the final sensor is currently ongoing. Two submissions labeled Engineering Run 2 (ER2) and Engineering Run 3 (ER3) are in the planning stage and their completion is expected in the second half of 2024 and 2025, respectively, and will include the full-scale sensors for the final system.

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