PROCEEDINGS OF SCIENCE

ATLAS ITk Pixel Detector Overview

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In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in up to 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of the ITk will consist of a pixel detector, with an active area of about 13 m^2. To deal with the changing requirements in terms of radiation hardness, power dissipation and production yield, several silicon sensor technologies equipped with novel ASICs connected by bump-bonding technique will be employed in the five barrel and endcap layers. As a timeline, it is facing to production of components, sensor, building modules, mechanical structures and services. This contribution presents the status of the ITk-pixel project focusing on the biggest challenges towards its production and operation, and it summarizes the latest results on developing closest-to-real demonstrator prototypes.

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1. Introduction

During the long shut-down 3 starting in 2026, the current ATLAS Large Hadron Collider (LHC) will be upgraded to the High Luminosity LHC (HL-LHC) leading to an substantial increase of the average pile-up from ≈ 60 to up to 200 proton-proton collisions at 40 MHz (25 ns bunch crossing). Data generation is estimated to reach 4000 fb^{-1} in 10 years of operation, starting in 2029 [1]. In order to meet these requirements, the current inner detector will be upgraded to an all-silicon tracker, called the Inner Tracker (ITk). The ATLAS-ITk consists of two sub-systems: a strip part [2] in the outermost layers and a pixel part [3] in the innermost layers close to the interaction point.

This work will focus on the development efforts targeting only the ITk-Pixel detector part. For this, the overall structure of the ITk-pixel detector will be presented before giving some details about its building blocks and the adopted technological solutions. Efforts to optimize the material budget will be summarized with few selected aspects to give an idea about the involved challenges, including the design, production and testing use cases.

2. ITk-Pixel Detector

The ITk-Pixel detector is composed of five layers (L0 to L4), covering a pseudo-rapitiy up to η = 4, as shown in Figure 1. The layers can be clustered in three different regions: The 2 innermost layers form the Inner System (IS), the other 3 cover the Outer Barrel (OB) in the center and the 2 Outer Endcaps (OEs). About 9700 modules are needed to cover the total 13 m^2 area of these layers.

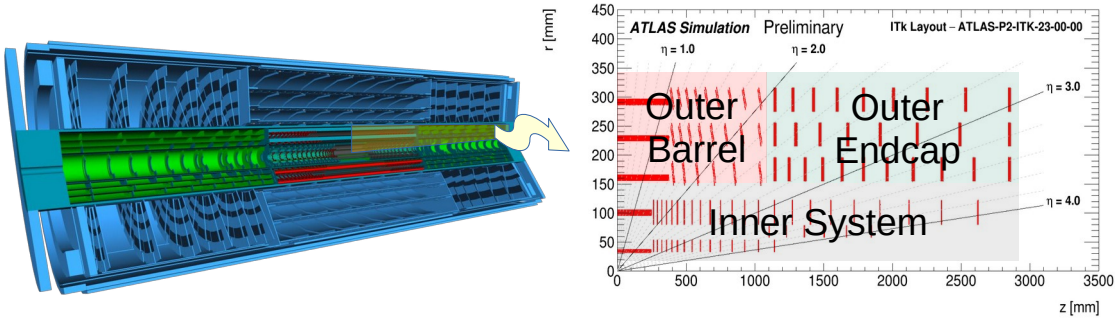

Figure 1: ITk layout (left) showing the strip and pixel sub-systems. Layout of (a quarter of) ITk-Pixel detector (right).

2.1 Sensors and Modules

To build a module, a sensor is bump-bonded to one or more readout Front-End (FE) chips. Different sensor architecture types (3-D or n-in-p planar), thicknesses (100 μm or 150 μm) and assemby configurations have been adopted. The combination (bare module) is then glued on a Flexible Printed Circuit (FPC), before wire-bonding to provide the required electrical connections. Modules are mounted on local support structures equipped with cooling pipes to keep the temperature at around -40°C during the ITk operation. Figure 2 shows an example of the quad-module (QM), using planar n-in-p 40x40 mm^2 sensor tile with 4 FE 20x20 mm^2 chips.

QMs, with 100 µm thick sensors, are used in the IS layer L1, whereas QMs in layers L2, L3, L4 of the outer Barrel and Endcaps will have 150 µm sensors.

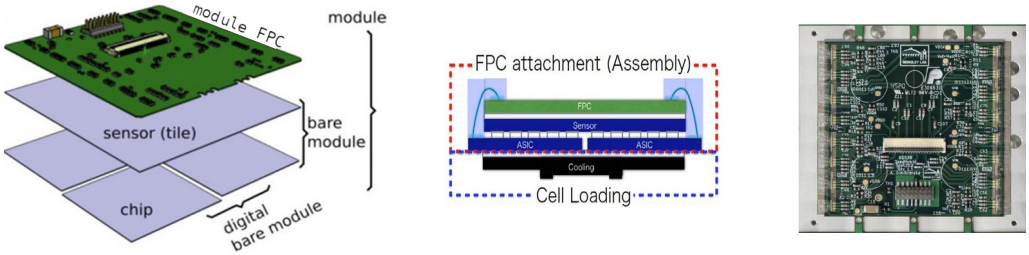

Figure 2: QM structure (left), loaded QM cross-section (middle) and one assembled QM photo (right).

For the IS layer L0, single modules (SM), organized in triplets are used. For each module one 3-D sensor is bump-bonded to one FE (both of 20x20 mm^2). 3 SMs are glued and wire bonded on an FPC, forming a so-called triplet as shown in Figure 3. It is foreseen that the IS modules of layers L0 and L1 would be replaced after 5 years of data collection as the total fluence would be around $10^{16}\,n_{eq}\,cm^{-2}$ @2000 fb^{-1}.

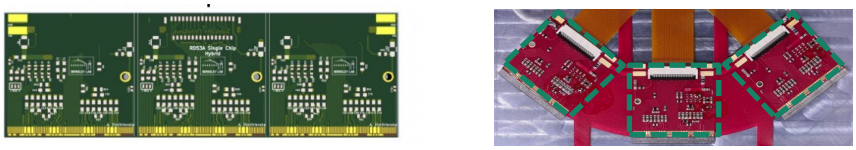

Figure 3: SMs arranged in triplet for L0 barrel (left) and for L0 ring (right).

2.2 Qualification and Testing

After a market survey to qualify the vendors involved in different production and/or assembly stages, a long-list of testing procedures and qualification is required to make sure that the built modules and the ITk-Pixel detector sub-systems meet the expected performance. In particular, for modules, testing during prototyping (using RD53A FE ASICs) and pre-production (using ITkPixV1 ASICs) includes thermal cycling done to stress the bumps, as well as electrical tests also performed to verify the module correct functioning. During this stage, design validation includes also the evaluation of module efficiency and track reconstruction, for un-irradiated and irradiated modules. This is usually done in testbeam campaigns.

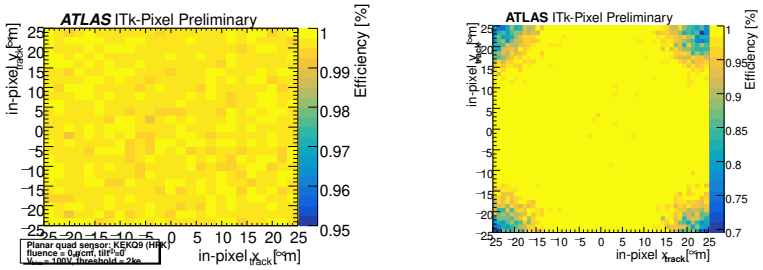

Figure 4: Example of testbeam measured in-pixel efficiency for un-irradiated planar ITkPixV1 QM (left) and un-irradiated 3-D SM (right).

In fact, it is required to obtain an in-pixel efficiency of 98,5% for un-irradiated and 97% for irradiated planar QMs. For 3D modules, the required in-pixel efficiency is of 96%. Figure 4 shows an example of achieved performance obtained with ITkPixV1 un-irradiated and

irradiated modules [4]. This test was done at CERN – Super Proton Synchrotron (SPS) in the Prevessin north area, using Pion beam at 120 GeV on a Mimosa26 telescope. The target in-pixel efficiency for un-irradiated and irradiated planar QMs are met, whereas, for 3D modules, the in-pixel efficiency near the p+ electrode region drops to 85% and 70%, while outside it reaches 100%. The average effeciency requirement is thus largely met.

During the production stage (with ITkPixV2 ASICs), a well documented quality control (QC) procedure is to be carried out for each module built, in order to be sure to install only good modules [5]. The site qualification of the involved institutes throughout the ATLAS collaboration is currently ongoing, in preparation for the actual production of the 9700 ITk-Pixel modules.

3. Towards System Production

Although the ITk-Pixel upgrade implies increasing detection surface, granularity and performance, the required material budget was reduced and greatly optimized. This was done through adopting carbon local supports for mechanical stability and mounting, CO2 cooling with thin Titanium pipes to minimize mass and maximize thermal performance. Loaded Local Support (LLS) and other sub-system demonstrators were built to validate the design choices, as shown in Figure 5.

Figure 5: ITk-Pixel LLS prototype examples for IS ring and OB demonstrator.

For the active parts, thin Si sensors and enhanced FE-chips were used. Advanced powering scheme (serial powering) was adopted to reduce cabling requirement for power connections [6]. The number of readout cables was also reduced using link sharing included in the FE ASIC design (ITkPixV1, ITkPixV2), and also via the aggregation of several commands and data links into one high-speed connection (lpGBT ASIC) and optical transceivers (VTRX+ ASIC).

Another domain of the upgrade development concerns the Data Aquisition (DAQ) system. Figure 6 depicts the schematic of one slice of the ITk-Pixel DAQ readout chain [7]. The off-detector part has, in its minimal configuration, a PC sever hosting a dedicated PCIe FPGA-based board (FELIX) that provides the interface between the back-end DAQ software and database on one side, and the on-detector hardware, on the other side. The DAQ software (ITkSW) sends configuration and control commands to the detector modules through FELIX, that transforms the signals from electrical into optical to the on-detector optobox. The latter will convert back into a 2.56 Gbps high-speed electrical signals (down-link) that are distributed through lpGBT aggregator ASICs to the corresponding FEs though 160 Mbps e-link connections. Hit data produced at the FEs are output at 1.28 Gbps data rate to the connected lpGBT that aggregates several of them into one high-speed up-link running at 10.24 Gbps, that will be converted into optical signal at the optobox, to arrive back in FELIX and then to the ITkSW software.

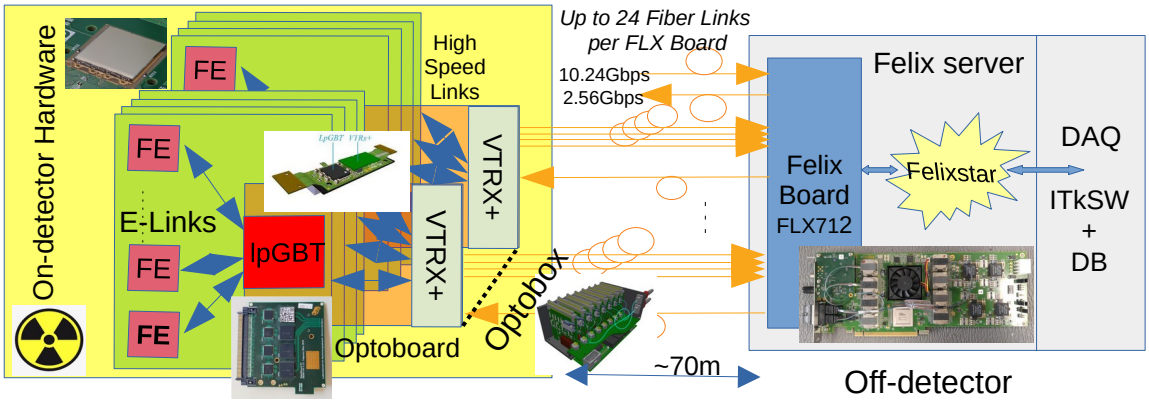

Figure 6: ITk-Pixel DAQ readout chain.

The overall functioning of the DAQ readout chain was validated on small scale laboratoy setups and work is ongoing to scale up the system, first in LLS sub-system demonstrator setups, arriving then to the full-scale DAQ system test.

4. Conclusion and Outlook

The ATLAS ITk is an all silicon detector replacing the current inner detector. It is composed of strips and pixel systems, to cope with the luminosity increasing with HL-LHC phase II upgrade. The ITk-Pixel detector is reaching an extensive prototyping and pre-production phase preparing the transition into production, expected to start by the end of 2024. System tests and demonstrators for all sub-systems are progressing well. The delivery of the final production version readout chip ITkPixV2 has already started and other services, loading and integration procedures are being finalized. All ATLAS ITk-Pixel collaboration member institutes are about to pass from pre-production into production phase to have upgraded ITk installed and operational by 2029.

References

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