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Evaluating Low-Precision Floating-Point Formats for Next-Generation Radio Telescope Correlators and Beamformers: A Quantitative Analysis of Linearity and Dynamic Range

Thushara Kanchana Gunaratne[a] **and Nicholas Bruce**[a,*]

[a] *Herzberg Astronomy and Astrophysics Research Center, National Research Council Canada Dominion Radio Astrophysical Observatory, 717, White Lake Road, Penticton, British Columbia*

E-mail: Thushara.Gunaratne@nrc-cnrc.gc.ca, Nicholas.Bruce@nrc-cnrc.gc.ca

The global environment for Radio Frequency Interference (RFI) is worsening, compelling the next generation of radio telescopes to incorporate resilient designs and implementations. While advances in telecommunications and consumer electronics have led to widespread deployment of such systems resulting in more RFI, they have also contributed to significant improvements in the receiver and processing capabilities of radio telescopes. This is especially significant for the digital signal processing (DSP) systems in the correlators and beamformers of radio telescopes. In an environment filled with strong and pervasive RFI, internal signal chains must support a high dynamic range while maintaining linearity. The floating-point number format allows for a high dynamic range, though it does so at the expense of precision. Prompted by the AI revolution, leading hardware vendors such as Intel-Altera, AMD-Xilinx, and NVIDIA are providing fast and efficient hardware implementations for low-precision floating-point arithmetic in their latest Field Programmable Gate Arrays (FPGAs) and Graphics Processing Units (GPUs). In this paper, we present an analysis of the linearity and dynamic range achieved by implementing key signal processing modules in the Square Kilometre Array (SKA) Mid-Frequency Correlator and Beamformer (Mid.CBF) using low-precision floating-point formats such as float16 and float32.

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1. Introduction

The global Radio Frequency Interference (RFI) environment is deteriorating, affecting even the most remote and sparsely populated regions that were prime candidates for radio telescopes [1]. This decline is largely due to the proliferation of ubiquitous terrestrial wireless communications systems and thousands of satellites providing communication, broadcasting, sensing, and navigation services [2]. Recently, the wireless communication industry has been pushing for the allocation of spectrum frequencies beyond 100 GHz, which were traditionally reserved for radio astronomy and other passive observations, for both terrestrial and space communications [3, 4]. This will further exacerbate the impact of RFI on existing and future radio telescopes. Given these challenges, it is crucial to explore other RFI mitigation strategies that enable the next-generation highly sensitive radio telescopes to coexist with strong and ubiquitous RFI.

One of the primary goals of radio telescopes is to achieve high dynamic range observations across a wider spectrum. The Square Kilometre Array telescope, currently under construction in its first phase, is expected to achieve an image dynamic range of 1 : 1,000,000 [5]. In order to achieve such a high dynamic range, concerted efforts are needed to enhance the performances for all key elements such as antennas, feeds, receivers, clock distribution networks, digitizers and the correlator and the beamformer to capture and process the weak celestial signals [6]. However, in the following we limit our study to the digital signal processing (DSP) carried out in the correlator and the beamformer (CBF) for the Mid-frequency telescope (SKA-Mid) using the signal-processing model specified in [7].

The SKA-Mid.CBF supports multiple observation modes, including normal and zoom imaging, pulsar search and pulsar timing beamforming, and VLBI beamforming and calibration. The functional architecture for the SK Mid.CBF is illustrated in Figure 1. The key signal processing modules of the Mid.CBF includes channelizers, which segment the observed bandwidth uniformly; resamplers to correct for propagation delays; tunable filters, which select specific regions of the sampled bandwidth; and beamformers and cross-correlators, which enhance the weak celestial signals. Further analysis shows that just two types of basic arithmetic operations are used in implementing these signal processing blocks. Those are a) the multiply and accumulate arithmetic operations that used in finite impulse response (FIR) filters and b) the cascading multiplier-adder chains used in the Fast Fourier Transforms (FFTs). The key to achieve high dynamic range in the SKA Mid.CBF is to maintain linearity in these basic arithmetic operations.

With the growing adoption of Graphical Processing Units (GPUs) and Field Programmable Gate Arrays (FPGAs) for Artificial Intelligence (AI) applications, leading hardware vendors such as NVIDIA for their latest GPUs [8] and Intel for their Agilex series FPGAs [9] have started providing 'native' support with 'hardened firmware-blocks' for the standard IEEE 754 single-precision (SP32) and half-precision (HP16) formats, along with different variants of those formats. Altera's Agilex Variable Precision DSP Block includes 'Fused Multiply and Accumulate' (FMA) functionality for HP16 and its variants (such as bfloat16 and bfloat16+), which helps maintain accuracy for partial sums [9]. Additionally, Altera provides 'Floating-Point IP Cores' for some of their Agilex, Stratix, Arria, and Cyclone series FPGAs that accommodate both standard IEEE 754 double-precision (DP64) and SP32 formats. Conversely, AMD-Xilinx presents configurable 'Floating-Point Operator' firmware blocks that support standard IEEE 754 DP64, SP32, and HP16

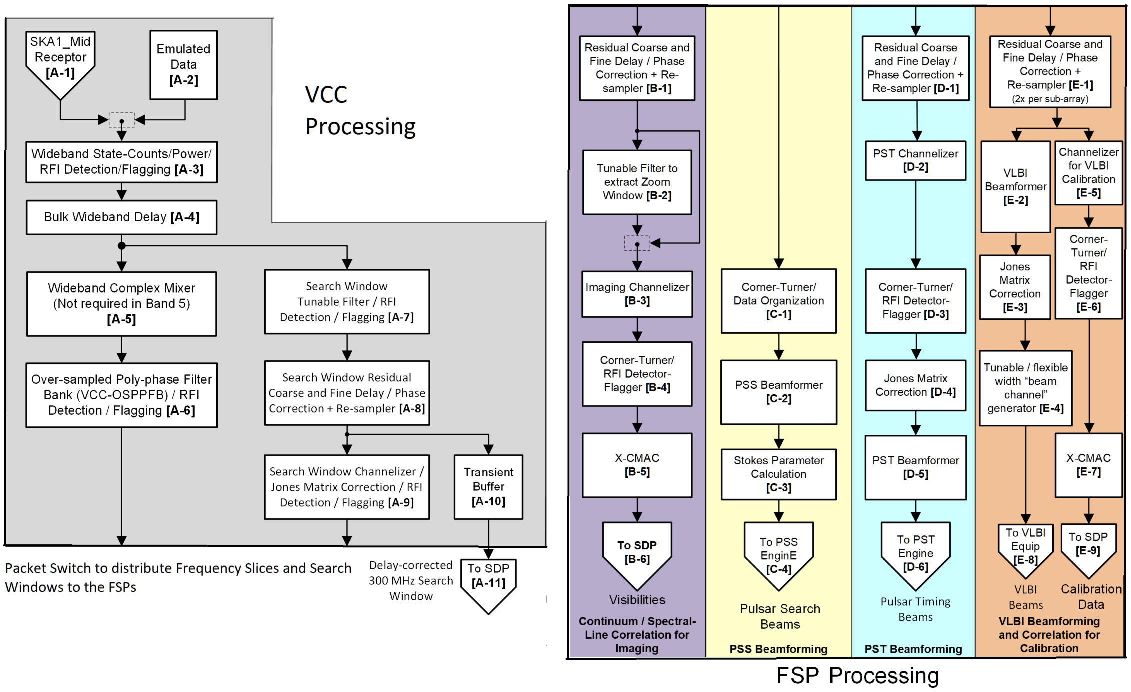

Figure 1: The functional architecture of SKA Mid CBF showing the key signal processing modules for different observing modes [7].

formats, respectively [10]. A variety of floating-point formats that are supported by NVIDIA in their GPUs along with Intel-Altera and AMD-Xilinx in their FPGAs, are listed in Table 1.

2. The Simulation Study

We conducted a numerical simulation study to evaluate the performance of the signal processing chains of SKA Mid.CBF implemented with fixed-point, HP16 and SP32 formats. In a previous study [11], we observed that the bfloat16 format does not have the dynamic range to achieve the required magnitude transfer responses for the key signal processing elements of the SKA Mid.CBF. We used the end-to-end simulation setup as outlined in Section 4.1 of [7], where the same test vectors are processed by two "functionally-identical" signal chains; one implemented with "double-precision" floating point arithmetic, which is considered the "Golden reference" and the other signal chain is implemented with either the fixed-point or HP16 or SP32. Note that the proposed architecture for the Mid.CBF mainly utilizes 19x18-bit fixed-point multipliers. However, in implementing a 16,384-point IFFT for the Imaging Channelizer, 27x27-bit multipliers had to be used in intermediate stages to maintain linearity. Similarly, for the HP16 implementation, the internal stages used the higher-precision SP32 format to maintain linearity.

In the test setup, the synthesized test vectors corresponding to two antennas separated by a 10 km baseline are first processed by the Very Coarse Channelizer (VCC), segmenting the input spectrum into "Frequency-Slices" (FSs) of ~ 200 MHz of bandwidth. Next, these FSs are processed by the resamplers to correct for propagation delays and associated phase-variations and then processed by the Imaging-Channelizer resulting in "Imaging-Channels" of width 13,440 Hz. Finally, the time

Manufacturer	Supported Formats	Details
NVIDIA [8]	float16 (HP16) bfloat16 tensor-float32 float32 (SP32)	Standard IEEE-754 (1S: 5E: 10M) Non-standard (1S: 8E: 7M) Non-standard (1S: 8E: 10M) Standard IEEE-754 (1S: 8E: 23M)
Intel-Altera [9]	float16 (FP16) bfloat16 float16+ or bfloat16+ float32 (SP32)	Standard IEEE-754 (1S: 5E: 10M) Non-standard (1S: 8E: 7M) Non-standard internal format (1S: 8E: 10M) Standard IEEE-754 (1S: 8E: 23M)
AMD-Xilinx [10]	half (HP16) single (SP32)	Standard IEEE-754 (1S: 5E: 10M) Standard IEEE-754 (1S: 8E: 23M)

Table 1: The low-precision floating-point formats supported in NVIDIA GPUs and Intel-Altera and AMD-Xilinx FPGAs.

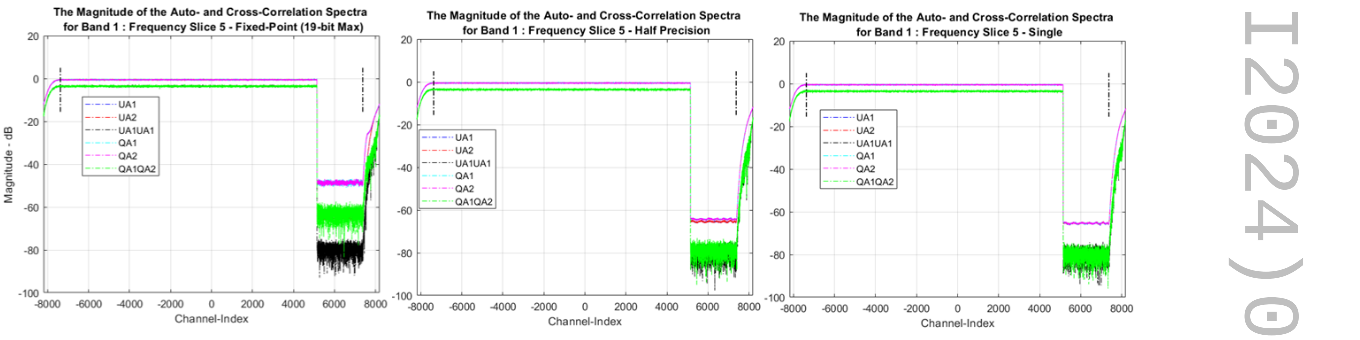

Figure 2: The auto and cross correlations for Frequency Slice 5 for SKA Mid.CBF achieved with signal chains implemented with DP64 (UA), 19-bit fixed-point (left) and floating-point formats HP16 (middle) and SP32 (right), respectively (QA).

series of the channels are self- and cross- multiplied and accumulated to evaluate the auto- and cross- correlations shown in Figure 2. As shown there the upper 12% of the spectrum in the 5th FS is devoid of any signal or noise allowing us to evaluate the dynamic range and linearity. The fact that the auto- and cross- correlation signal levels in this part of the spectrum are below -60 dB and have no spurious components when compared with the rest of the spectrum, indicates that all three implementations attained greater than 60 dB dynamic range while maintaining linearity.

3. Conclusions

The RFI environment is fast deteriorating all over the world. There are few alternatives other than increasing the dynamic range while maintaining the linearity of the signal chain for radio telescopes. Fortunately, mainstream vendors are now supporting low-precision floating point arithmetic operations natively. A preliminary quantitative study was conducted to evaluate the imaging signal chain for the SKA Mid.CBF with the HP16 and SP32 floating point formats against the currently proposed fixed-point representation and the golden reference of DP64 formats. It has been observed that for HP16 and fixed-point implementations, the signals in the intermediate stages of the long IFFTs must be represented with higher precision to maintain linearity. With this caveat, it is possible to implement the SKA Mid.CBF with FP16 and achieve the desired sensitivity whereas SP32 implementation would yield a slight increase in sensitivity but, at a much greater computational cost. In the future, we plan to conduct similar studies for other observation modes of the Mid.CBF.

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