PROCEEDINGS OF SCIENCE

DRS4 based SiPM readout electronics for the Cosmic Muon Veto Detector at IICHEP

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A cosmic muon veto detector (CMVD) is being built around the mini-ICAL detector which is operational at IICHEP, Madurai. It will study the feasibility of building a shallow depth neutrino detector. It's being built using extruded plastic scintillator (EPS) strips. Muon interactions in the EPS are detected by SiPMs mounted at the end of 2 wavelength shifting fibres which are inserted in the EPS strips.

The muon detection efficiency of the CMVD is required to be more than 99.99%. Faithful detection of muons requires SiPM charge measurement. SiPM signals are converted to voltage pulses by trans-impedance amplifiers. A DRS4 based readout system is being designed to sample the signals at a rate of 1 GS/s. The samples are digitized on receiving a mini-ICAL trigger, and zero-suppressed data are transmitted to the back-end data server. An FPGA based DAQ board consisting of 5 DRS4 ASICs and a network interface is being designed. This paper will discuss the prototype design of the SiPM readout board.

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1. DRS4 for SiPM Charge Measurement in the CMVD DAQ

Charge measurement of muon signals generated by SiPMs requires the DAQ to integrate the signal for a specific time, depending on the pulse profile, after identifying the arrival of a muon through a trigger. This is a tricky situation, as the muon signal, which is used to generate a trigger, is already lost due to the trigger generation delay - the trigger latency. Provided enough data bandwidth is available, digitizing a signal for a wide enough window enables us to do this. This can be achieved with the DRS4 chip.

A typical SiPM signal for a muon, after amplification, has a rise time of 8-10 ns, an amplitude of 10-1000 mV and a pulse opening of up to 150 ns. A pulse with 8 ns rise-time can be reliably sampled at a frequency of 1 GHz, and with 1024 cells, a DRS4 channel can store pulse profile for the last 1024 ns. This is long enough to accommodate a trigger latency of 300 ns plus pulse profile time of 300 ns. DRS4 can accept input voltage up to a volt, and using an ADC with enough bits, one can gain full dynamic range required to cover the full spectrum of the muon pulse amplitudes at the required least count.

2. Principle of Operation

The DAQ system must measure and store the value of the charge produced by every relevant SiPM in the CMVD on every mini-CIAL trigger. To do this, we use the DRS4 chip to sample the SiPM signal. The DRS4 is a switched capacitor array which can sample 8 input channels at up to 5 GSa/s and store the input analog waveform in 1024 cells per channel. Whenever required, the DRS4 can be stopped to readout this stored waveform for external digitization. Thus, at any point of time we can readout the last 1024 ns of the analog waveform if we are sampling the input channels at 1 GSa/s.

Upon a mini-ICAL trigger, the DAQ boards will stop the DRS4 sampling process and readout the stored waveform for digitization, so that the status of the SiPM during the trigger can be read and stored if found relevant. Since the trigger latency can be measured, the DAQ can readout only the region of interest (ROI) from the 1024 ns of the stored waveform. The ROI will be adjusted to have the full pulse width of the SiPM signal for a typical muon event, plus some overhead to accommodate the jitter owing to the 4.7 m long plastic scintillator, the trigger latency, and some part of the waveform before the pulse to determine any baseline offset. The stored digitized data will be processed online in the FPGA to perform baseline offset correction and zero suppression to reduce the data size. It can be further processed to find the charge value of the SiPM pulse to reduce the data size by a factor of about 100.

3. DRS4 Based DAQ board for the CMVD

Figure 1 shows the block diagram of a DAQ board based on DRS4 for the CMVD. A prototype board has been made around a Xilinx Spartan-7 FPGA. The final DAQ board will cater to 40 SiPM channels and will therefore incorporate 5 DRS4 chips. The front-end is a transimpedance amplifier with a common-base transistor front followed by an op-amp stage.

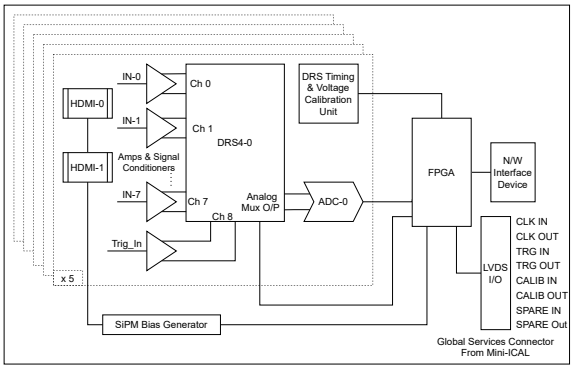

Figure 1: DRS4 based SiPM-DAQ Board Block Diagram for the CMVD

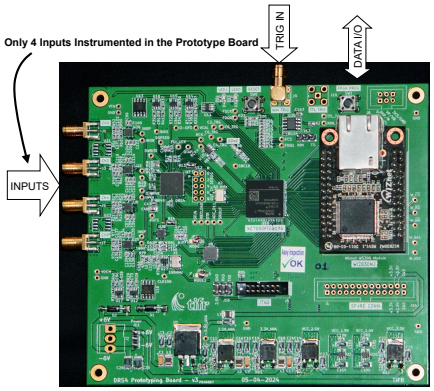

Figure 2: Prototype DRS4 based DAQ Board using a Xilinx Spartan-7 FPGA

4. Results

We have successfully tested the prototype DAQ board. We are able to perform calibration of the inherent offsets in the cells of all the DRS4 channels. Figure 3 shows the offset values for all 1024 cells in channel 3 of DRS4. A tailpulse captured in ROI readout mode from DRS4 can be seen in Figure 4.

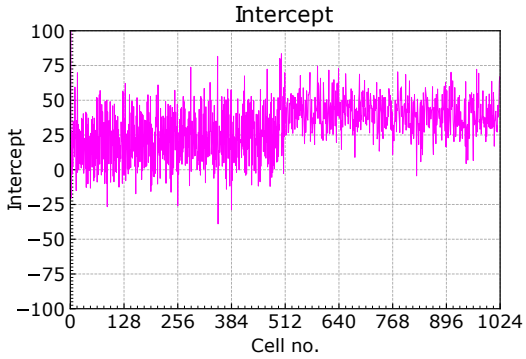

Figure 3: DRS4 Calibration: Intercepts for all 1024 cells of a channel

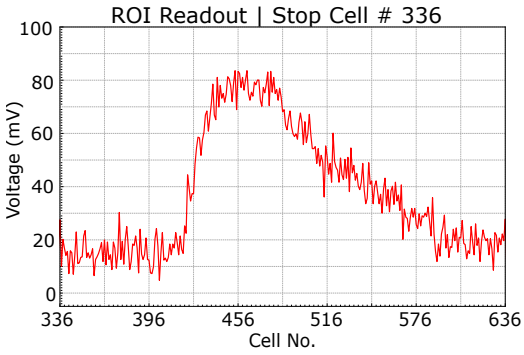

Figure 4: A tail pulse recorded in ROI mode with ROI = 300 ns

5. Further Work

The prototype board is working successfully. This work can now be expanded to the final DAQ board, which will have 5 DRS4 chips to read out 40 SiPMs. About 78 such boards will be required for the full instrumentation of the CMVD.

References

[1] M. Saraf, S. R. Bharathi, S. Bheesette, *et al.* "Overview of the Cosmic Muon Veto Detector for the Mini-ICAL at IICHEP, Madurai," Springer Proc. Phys. **304** (2024), 298-302 doi:10.1007/978-981-97-0289-3_65