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Liquid-based micro-channeling for efficient FPGA cooling

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FPGA devices offer interesting solutions for boosting the real-time processing capability of HEP experiments but efficiently dissipating heat is a challenge particularly for the coming dense and high-performance computing systems. Liquid-based cooling is a promising technology for offering a compact and energy-efficient cooling system. We designed, constructed and tested prototypes for liquid-based cooling based on micro-channels etched on silicon wafers. The first batch of prototypes was recently completed at FBK in Trento and tested at INFN laboratories. Preliminary results, confirmed by simulation based on computational fluid dynamics, obtained a heat dissipation capacity of ~6 W/cm^2, competitive with traditional heat dissipation methods.

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The thermal dissipation of electronic components with liquid-based cooling traversing micro-channels nearby where transistors operate is an attracting avenue of exploration for scaling up the density and computational power in high-performance computing systems [1, 2]. This is particularly attractive for the future trigger and data acquisition systems of HEP experiments, where dedicated computing accelerators, such as FPGAs, will be performing dedicated and intensive algorithmic tasks. Liquid-based cooling with micro-channels offers a high surface-over-volume ratio, low thermal resistance between the fluid and the circuit dissipating power and overall a promising R&D for FPGA cooling for future HEP experiments.

A first micro-channel layout has been designed, as depicted on the left of Figure 1, and different prototypes have been constructed at FBK in Trento. The prototypes are on silicon wafers with a 625-μm thickness. The micro-channels have been etched with three different depths, corresponding to 200, 250 and 300 μm. Such wafers have been bonded with anodic procedure with a second silicon-based or pyrex-based layer to effectively close the micro-channels and eliminating the need to directly flow the cooling liquid on the die where the functional components are fabricated.

Load and breaking tests at INFN laboratories demonstrated some fragility for the silicon-silicon double-layer solution. The best operational performance was obtained by the silicon-pyrex combination with micro-channels with a 300-μm depth, which have then been used for dedicated thermal tests. The prototypes have been coupled with thermal resistors with a thermally conductive glue and connected with dedicated peeks, as shown on the right of Figure 1.

The experimental setup consisted of a cooling circuit with a Novec 7100 liquid refrigerated at 5 °C and a mass flow rate of 0.33 kg/min in a room with a constant temperature of 21 °C and relative humidity of 51%. The measured liquid pressure at the entrance of the micro-channels was 3.42 bar. The thermal resistors have been set with ranging values of voltage and current for testing dissipation power within the range $1 - 6$ W/cm^2. The most demanding thermal management configuration was measured to be 97.1 W, corresponding to ~6 W/cm^2. An infrared camera measured the temperatures at different points within the thermal resistor. The measured temperatures when injecting 97.1 W were within $65 - 80$°C, as shown on the left of Figure 2 and stable over time.

A simulation based on computational fluid dynamics was also developed. The simulation model consisted of roughly 7M cells and, using a conjugate solid and liquid heat-transfer model, the simulated temperatures confirmed the experimental results, are shown on the right of Figure 2. Such simulation has been used to vary the geometry of the design and a second configuration, with a more regular pattern of micro-channels over the entire surface to be cooled, has been achieved. Such second design will be constructed at FBK for further tests. The achieved performance of ~6 W/cm^2 is already considered an interesting achievement, but both the experimental setup and the related simulation suggest that a higher power dissipation per unit area could be achieved with this technology.

Acknowledgments

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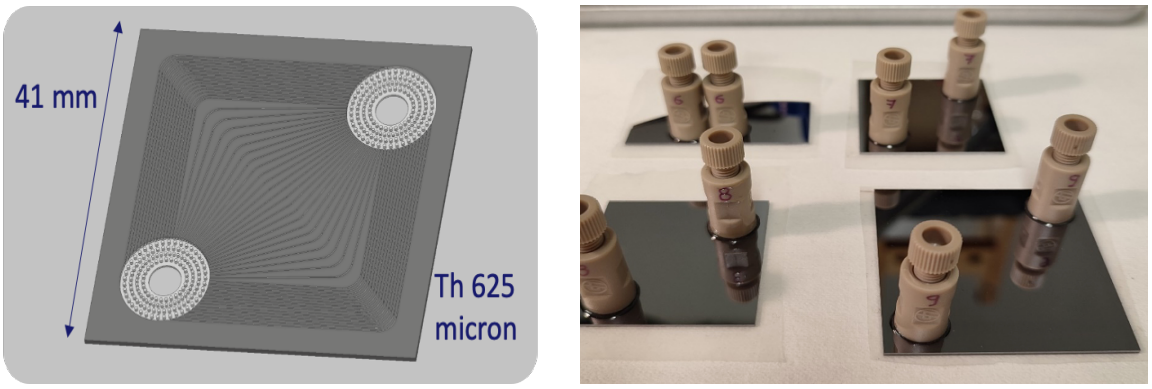

Figure 1: (Left) Design of the constructed micro-channel configuration on a 41x41 mm^2 silicon square. (Right) Final prototypes with silicon-silicon double layer with a thickness of 625 + 450 μm.

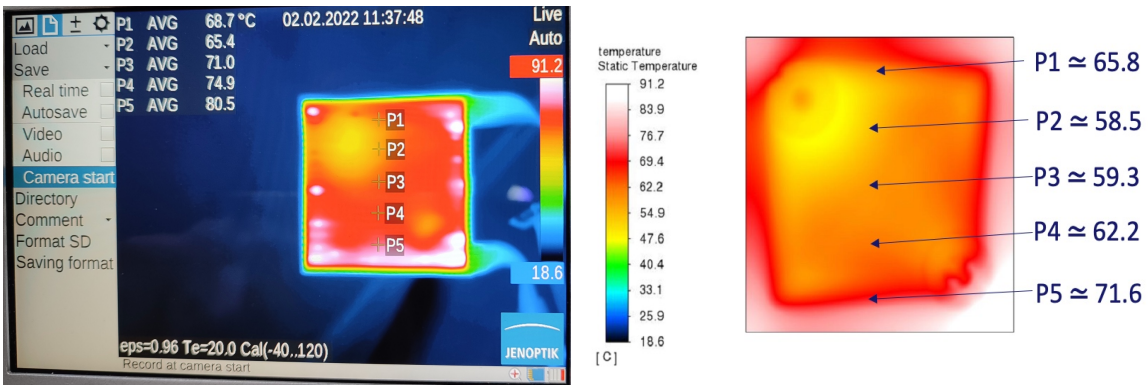

Figure 2: (Left) Measured temperatures in five different points and related heat map when injecting 97.1 W into the thermal resistor and cooling it down with the developed liquid-based micro-channeling system. (Right) Simulated temperatures corresponding to the same experimental setup confirming the results.

References

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