PROCEEDINGS OF SCIENCE

System tests with the TEPX detector for the CMS Inner Tracker upgrade

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The upcoming High-Luminosity Large Hadron Collider (HL-LHC) upgrade will allow the CMS experiment to collect up to ten times the integrated luminosity than that provided by the baseline program. The CMS detector will undergo significant upgrades to handle the increased data rates and harsher operational conditions expected in the HL-LHC era with its inner tracker system completely replaced. The endcap of the upgraded inner tracker, the Tracker Endcap Pixel (TEPX) sub-detector, is composed of four disks at either end. Each double disk employs four different printed circuit boards (PCBs), hosting the TEPX modules. To reduce material and cabling, the disk PCB has fewer readout data lanes in its outer rings, which is compatible with the lower hit rate in this region. In the outer rings, data from different readout chips in the same module are merged into the primary chip. In this contribution, the final design of the TEPX disk PCB is evaluated by testing the modules on different positions of the PCB. The performance of the data merging feature of the TEPX module is also compared and validated with its normal data readout scheme.

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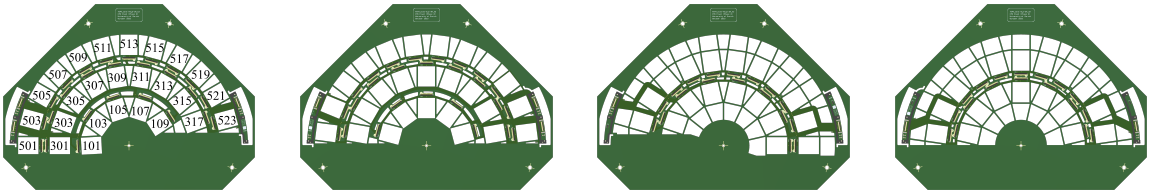
1. The Phase-2 Upgrade of the CMS Inner Tracker

The upcoming High-Luminosity LHC (HL-LHC) upgrade [1] will enable more precise measurements and has the potential to observe rare processes that are not currently detectable. During the shutdown period following Run 3, CMS will undergo significant upgrades to handle the increased data rates and harsher operational conditions with its inner tracker system being completely replaced. The Phase 2 CMS Inner Tracker (IT) consists of the Tracker Barrel Pixel (TBPX), Tracker Forward Pixel (TFPX), and Tracker Endcap Pixel (TEPX) detectors. The TEPX detector has four disks at each of the two ends of the IT. It utilizes quad modules containing 2×2 CMS Read-Out Chips (CROCs) developed by the RD53 Collaboration [2]. The CROCs are bump-bonded to planar silicon sensors with a pixel size of $100 \times 25\ \mu\text{m}^2$ and wire-bonded to a High-Density Interconnect (HDI) printed circuit board (PCB). This paper briefly reports the validation of the TEPX disk PCB and the results of the data merging test with the CROC.

2. TEPX Disk PCB

The TEPX disk PCB hosts the mounted TEPX modules, providing data connections and serially distributing power supply and bias voltage [3]. There are four different layouts, as shown in Figure 1, with either a 2-ring or 3-ring structure. Each single disk is composed of a carbon foam layer enclosing titanium cooling pipes for distributing CO_2, sandwiched between two carbon fiber sheets, where two PCBs are glued together. The extra material of the PCBs (shown in green) is only for processing and will be removed before assembling them on the carbon fiber. The 2- and 3-ring PCBs complement each other's $|\eta|$ coverage, while the symmetric and asymmetric layouts provide full coverage in the azimuth angle $|\phi|$.



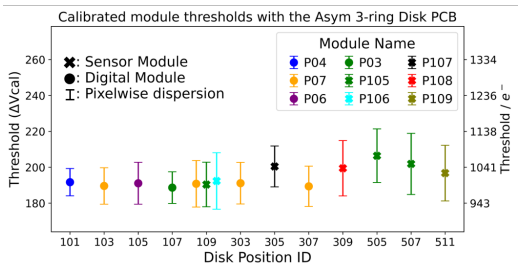
a. The asymmetric 3-ring layout. **b.** The symmetric 3-ring layout. **c.** The asymmetric 2-ring layout. **d.** The symmetric 2-ring layout.

Figure 1: The four layouts of the TEPX disk PCB.

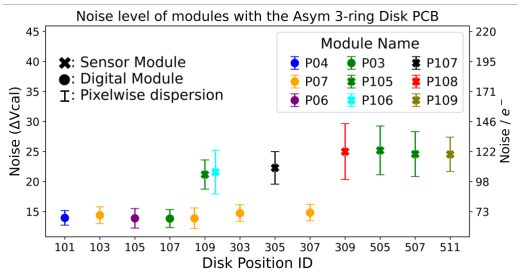
Due to the increased granularity and coverage of the new tracking system, the modules must be powered serially to avoid excessive cabling and material in the detector's innermost region. The performance of TEPX modules in a serial power chain has been verified and is consistent with tests using a standalone powering board [4–6]. Testing the modules on the disk PCB is important to ensure the PCB does not introduce additional noise.

In this paper, the test results of the asymmetric 3-ring disk PCB are included. The ID of each position is labelled in Figure (1a). The test uses both CROCv1 prototype modules with and without silicon sensors, which are denoted as "sensor modules" and "digital modules", respectively. The positions in the disk without modules are filled with bypasses to close the serial power chain. The modules are tested on different positions of the PCB, which is powered with a constant-current power supply of 8A. A high bias voltage of $-30\,\text{V}$ is applied for each single ring separately

when testing sensor modules. The data is read out through a flex cable connected to a port card with lpGBT chips and VTRx+ optoelectronic modules, converting the electronic signals to optical signals, which then are sent by optical fibers to the FC7 backend data acquisition board.



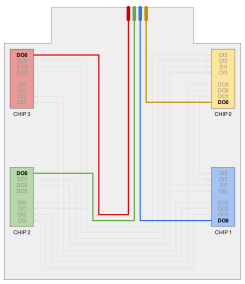
a. The mean value and standard deviation of the threshold distribution of different modules.



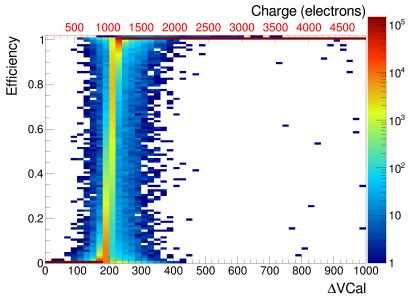
b. The mean value and standard deviation of the noise distribution of different modules.

Figure 2: The threshold and noise of different modules calibrated on the different positions of the asymmetric 3-ring disk PCB. The ID of each position is labelled in Figure (1a). The sensor modules are marked with cross markers and the digital modules with round markers. Position 109 is tested with three different modules.

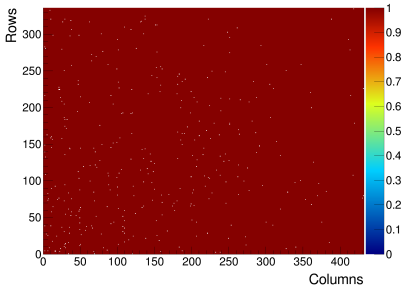
The modules are tuned to a threshold of 1000 e^- in the disk PCB. All calibration procedures work successfully with the PCB. An S-curve is obtained by measuring the hit efficiency while varying the charge of an injected calibration signal. The threshold of a pixel is defined as the charge where the efficiency is 50% and the noise as the difference between the values of the charges corresponding to 70% and 30% of the efficiency. The S-Curves are measured for all working CROCs on each module. The threshold and noise of a module are defined as the mean values of their respective distributions. The test results with the asymmetric 3-ring disk PCB are shown



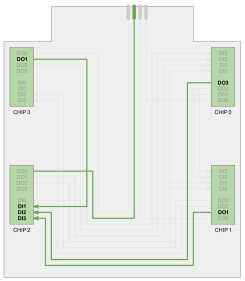
a. The normal readout scheme with 4 data lanes.



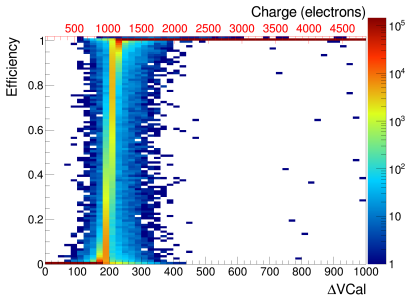
b. The S-curve of chip 3 measured with the normal readout scheme.



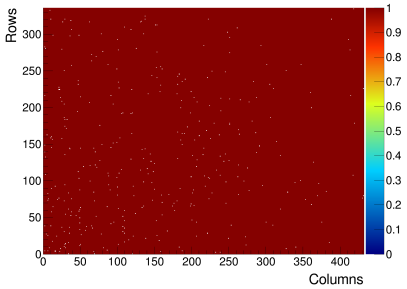
c. The scan of alive pixels of chip 3 with the normal readout scheme.



d. The data-merging scheme with 1 data lane.



e. The S-curve of chip 3 measured with the data-merging readout scheme.



f. The scan of alive pixels of chip 3 with the data-merging readout scheme.

Figure 3: Data merging test on the TEPX module.

in Figure 2, with Figure (2a) showing the mean value and standard deviation of the threshold distribution of different modules and Figure (2b) the noise results. The silicon sensor introduces an additional capacitance at the input of the corresponding chip channel and therefore additional noise to the module compared to the digital ones. The results show that the disk PCB features a consistent, low noise level across positions compared to the calibrated threshold. The results are also consistent with those from standalone tests without the disk PCB.

3. TEPX Module Data Merging Test with the CROC

As shown in Figure (1a), the number of modules hosted in the disk increases outwards because of the geometry, while the hit rate decreases away from the beamline. To reduce material and cabling, the disk PCB has fewer readout data lanes in its outer rings, which is compatible with the lower hit rate in the outer region. In the outer rings, data from different ROCs in the same module are merged through lines in the HDI, with different schemes in the four external rings. Command signals to the CROCs are also sent to the primary chip first and then delivered to others. Therefore, it is crucial to verify that the data merging works properly. As shown in Figure 3, chip 3 in a CROCv2 module is calibrated with the normal readout scheme shown in Figure (3a) and the data-merging scheme shown in Figure (3d) respectively. The results of the S-curve measurement and scan of alive pixels are compared between different schemes and are found to be consistent.

4. Summary

The different positions on the TEPX disk PCB for the CMS Phase-2 Inner Tracker Upgrade have been tested with different TEPX modules. The results show that the disk PCB features a consistent, low noise level across positions with respect to the calibrated threshold of the module. The data merging feature of the module was also tested and found to have consistent performance in comparison to the normal data readout scheme. The design has been finalized for all parts, and most items, like HDIs, disk mechanics and PCB, and port-cards are being procured. Module pre-production is ongoing and the first production disk will be available in the first half of 2025.

References

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[6] F. Stäger et al., *Performance of Phase-2 CMS Inner Tracker CROC-V1 modules in a serial power chain*, *PoS* **LHCP2023** (2024) 272.