PROCEEDINGS OF SCIENCE

Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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A new era of hadron collisions will begin around 2030 with the High-Luminosity Large Hadron Collider (HL-LHC), which will enable the collection of up to ten times more data than was recorded during the first decade of LHC operations. This performance will be achieved through a substantial increase in instantaneous luminosity, at the cost of a significantly higher number of proton-proton collisions per bunch crossing. To withstand the expected high radiation doses and challenging data-taking conditions, the ATLAS Liquid Argon (LAr) Calorimeter readout electronics are being upgraded. Additionally, the trigger rate of the first level trigger is projected to be increased to ten times its current rate. The new trigger system must be provided with higher granularity up to cell-level for the energy reconstruction. This proceeding presents an overview of the new hardware systems, the status of their development and production, and the ongoing integration tests that are preparing the upgraded LAr readout for operation at the HL-LHC.

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1. Introduction

The ATLAS [1] Liquid Argon (LAr) Calorimeter is a sampling detector with 182,468 cells arranged into multiple layers and divided into four main components: the Electromagnetic Barrel (EMB), the Electromagnetic End Cap (EMEC), the Forward Calorimeter (FCal) and the Hadronic Endcap (HEC). Using Liquid Argon as the active material and various metals (lead, copper, and tungsten) as absorbers, it measures the energy, position, and timing of particles through the ionization produced in electromagnetic showers. In the current configuration, two readout paths are used. The digital trigger path transmits reduced granularity data (≈34,000 supercells) every 25 ns to the trigger system. This feature was introduced during the first step (Phase-I [2]) of the upgrade, during the second LHC long shutdown (LS2). The data readout path is activated upon a positive trigger decision at rates of up to 110 kHz, providing the data recorded for offline analysis. With the High-Luminosity LHC (HL-LHC), the instantaneous luminosity is expected to increase by a factor of up to 7.5, reaching about 7.5×10^{34} cm^{-2}s^{-1}. This will lead to a higher number of proton-proton interactions per bunch crossing (from around 80 inelastic proton-proton collisions in the current run to about 200 at the HL-LHC), resulting in an increase in radiation, but also in pile-up conditions.

To cope with these conditions, the ATLAS LAr Calorimeter will retain its detector structure but will receive a replacement of its readout electronics, extending the already present Phase-I upgrade (see Figure 1). The new system will provide full detector granularity to the new trigger path and will undergo changes to support the increased trigger rate of up to 1 MHz.

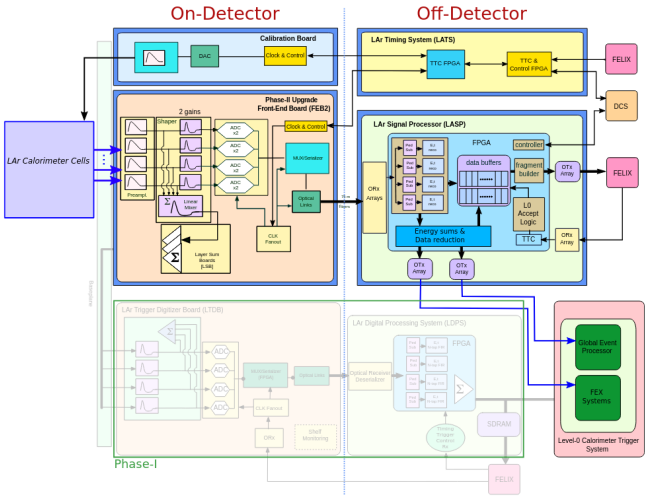

Figure 1: Plan of the LAr calorimeter on-detector and off-detector electronics for the HL-LHC. The systems shown on the upper half of the figure are going to be installed during the next LHC long shutdown (LS3), while the shaded one are already operational and were installed during the previous LHC long shutdown (LS2) [3]

The data chain is composed of four main components, divided between the on-detector electronics and the off-detector electronics. Their design, functionalities, and current development status are described in Section 2 and Section 3, while system integration and data tests are presented in Section 4.

2. On-detector Readout Electronics

Located near the collision point, the on-detector readout electronics must tolerate radiation levels of up to 4.1×10^{13} n_{eq}/cm^2 (Non-Ionizing Energy Loss) at 1.4 kGy (Total Ionization Dose) and maintain minimal error rate while operating under such conditions. The Front-End Board 2 (FEB2) amplifies, digitises, and transmits the signal of all calorimeter cells to the off-detector systems, corresponding to a total of $\approx$ 345 Tb/s of data sampled at 40 MHz, . The calibration board injects precise calibration pulses into the FEB2, ensuring high accuracy in signal amplitude and timing resolution. The calibration board should achieve a non-linearity below 0.1%, a non-uniformity below 0.25%, and a pulse rise time shorter than 1 ns while operating under the same radiation conditions.

2.1 Front-End Board 2 (FEB2)

Pre-amplification and shaping of the signal Custom ASIC chips, designed in 130 nm CMOS technology, are used to amplify and shape the incoming signal. Each chip handles four channels, corresponding to four calorimeter cells. The signals are first shaped and split before being amplified to produce two gain outputs with a gain ratio of 25. In addition, the analog sum of the 4 incoming channels is computed and propagated to a Layer Sum Board (LSB) that interfaces with the digital trigger path installed during the previous upgrade.

Two different types of ASICs will be used for analog signal pre-amplification and shaping. The ALFE chips are used for the EMB, the EMEC, and the FCAL regions. In the HEC, the amplifiers are located inside the cryostat, and the signal transmitted to the FEB2 requires only shaping. For this reason, a dedicated chip, the Hadronic Pre Shaper (HPS), is used, replacing the pre-amplification stage with a shaping function. To instrument the full detector, 80,000 chips will be produced, of which, 2,700 are HPS chips. Radiation qualification tests have been successfully completed, and all chips are currently undergoing characterization using automated robotic test benches before integration onto the FEB2.

Signal sampling The sampling of the signal is performed using custom ASIC chips, designed in 65 nm CMOS technology and known as COLUTA [6]. These chips digitise the output from the shaper for both gain channels at a rate of 40 MHz, providing an effective 14-bit dynamic range. The digitisation is achieved using a combination of 3-bit Multiplying DACs (MDAC) and 12-bit Successive Approximation Register (SAR). In addition to the sampled signal, timing information is recorded by including the bunch crossing ID (BCID) into a dedicated frame, ensuring synchronization of all channels in the subsequent stages of the readout chain. The digitised data are then transmitted to an lpGBT interface, which handles the optical data, serializes them, and transmits them to the off-detector electronics. Approximately 80,000 COLUTA chips will be produced. Radiation, vibration, and thermal qualification tests have been successfully completed. As with the amplifier and shaper ASICs, each COLUTA will undergo detailed characterization using dedicated robotic test benches before being installed on the FEB2.

Complete board All the aforementioned chips are assembled on the FEB2. Each FEB2 hosts 32 ALFE (or HPS) chips, 32 COLUTA chips, 24 lpGBT chips, and one mezzanine LSB, enabling the readout of data from 128 calorimeter cells per board. In total, 1524 FEB2 boards will be

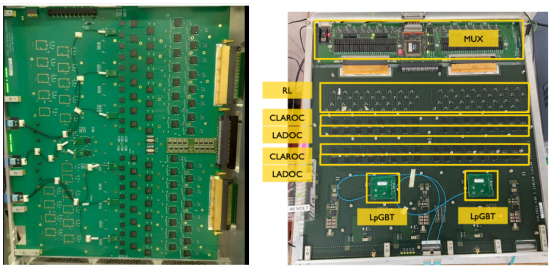

Figure 2: Pictures of the most recent prototype of on-detector board. On the left side is a FEB2v2.5. On the right side is a CABANEv1, the board implementation of the calibration board.

installed on the detector. Currently, a handful number of boards have been assembled and are undergoing performance testing. Studies on individual FEB2 boards have demonstrated pedestal stability, coherent and correlated noise level, pulse shape quality and linearity that are compliant with the board's design specifications.

2.2 Calibration board

Amplitude and timing of the pulse The calibration pulse is generated using two dedicated ASIC chips. The first, LADOC (with a 130 nm TMSC technology), provides a precise DC current source and is also used for slow control operations. The second, CLAROC (with a 180 nm CMOS technology), include a high frequency switch that opens upon receiving a command pulse. Together, these components, combined with a precise inductor and resistor, generate a well-defined calibration pulse with controlled amplitude and timing characteristics. Radiation qualification tests have been successfully completed, and the production of the final ASICs will begin shortly. Dedicated robotic setups are being prepared to characterize all chips before installation.

Complete board Each calibration boards hosts 32 LADOC and 32 CLAROC chips, enabling the generation of 128 calibrations channels with a 16-bit dynamic range. A total of 122 boards will be installed in the detector, each capable of pulsing 12 FEB2 simultaneously. A development prototype, called CASA, has been tested and included in integration tests (see Section 4). Preliminary tests of the CABANE prototype board, shown in Figure 2, are ongoing and will provide validation of the final design.

3. Off-detector

3.1 Liquid Argon Timing System (LATS)

The LATS system retransmits, via the lpGBT protocol, the clock, recovered from the Local Trigger Interface (LTI), to all the front-end electronics boards. Through this LTI protocol, precise timing information are transmitted to all boards and pulse-related information, such as the pulse command and the phase of calibration pulses, are transmitted to the calibration boards. Another key function of the LATS is the configuration and control of all 1524 FEB2s and 122 calibration boards. Each LATS module can monitor, control, and synchronize up to 72 boards via lpGBT connection.

The LATOURNETT board (the hardware implementation of the LATS, shown in Figure 3), contains 13 Intel® Cyclone10® GX FPGAs, organized into one Central FPGA and 12 matrix

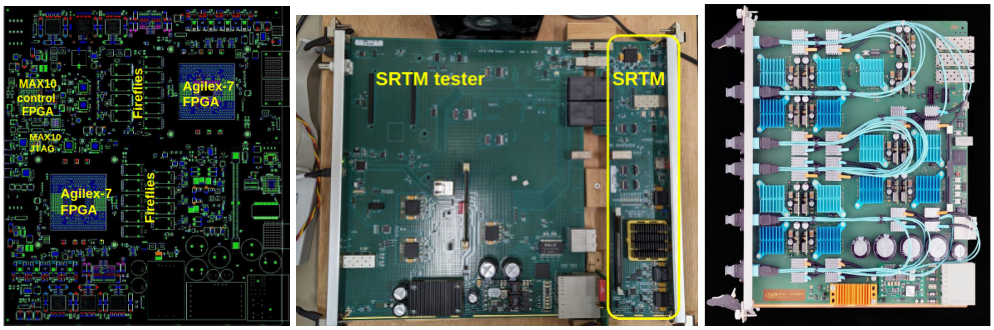

Figure 3: Pictures of the newest prototype of off-detector boards. On the left side is a LASP-T2 test board of the LASP. In the middle is a SRTM v2.0 with a SRTM test board simulating the LASP connection to the SRTM. On the right side is a LATOURNETTv1, the board implementation of the LATS.

FPGAs. The central FPGA, interfaces with a Gigabit Ethernet (GbE) connection, enabling slow-control monitoring and communication with the board. It also receives the TTC signal, which it then distributes to the matrix FPGAs. Each matrix FPGA interfaces with six front-end boards, propagating timing signals, transmitting monitoring and configuration data, and sending calibration pulse commands (for the Calibration board). Dedicated firmware is being developed for both the central and matrix FPGAs to support their respective functions.

The LATOURNETT prototype has successfully passed preliminary hardware qualification tests and is currently being integrated into the full test system setup (see in Section 4).

3.2 Liquid Argon Signal Processor system

The LASP is responsible for the time and energy reconstruction of the full granularity of the detector, corresponding to a total data throughput of approximately 345 Tb per second transmitted over 33000 links from the FEB2 at the 40 MHz collision rate. The processed data are first sent to the trigger system, then buffered while awaiting the trigger decision before being transmitted to the Data Acquisition (DAQ) system. The LASP system is composed of a main blade and a Smart Rear Transition Module (SRTM). The main blade contains two Intel® Agilex® 7 FPGA per blade, each receiving data from three FEB2s. The SRTM include a Xilinx® Zync® Ultrascale FPGA and interfaces with the LTI systems at 10 Gbps, as well as the trigger and DAQ output at 25 Gbps.

The LASP firmware must receive and synchronize data from three FEB2s, compute the cell-level energy and timing, and transmit the cell's energy to the global trigger system at 40 MHz. The data are then buffered until a 1 MHz rate trigger decision is received, after which the full dataset is sent to the DAQ system. To perform energy and time reconstruction, new Optimal Filtering techniques are under development and testing.

The first prototype of the LASP boards are currently being build. Planned test activities include dedicated test benches, full specification verification, and integration with the SRTM modules. The firmware is being developed and being tested on an earlier version of the board in an integration setup at CERN presented in Section 4.

4. Integration

An integration setup is being developed at CERN to test the interoperability of all the modules described in the previous sections. This setup is designed to closely reproduce the final hardware configuration and operating connections expected during the HL-LHC operations. It enables the validation of hardware and firmware interconnections, communication protocols, and system-level interactions. In addition, it supports the development and testing of online software used for monitoring, control, and safety verification. Having all components integrated in this setup also allows the establishment of a complete data acquisition chain, from the on-detector to the off-detector systems. This provides an essential platform for testing the offline software, which is responsible for the reconstruction and analysis of the recorded data.

The diagram of the LAr Phase-II integration setup is presented in Figure 4. The ALTI [8] and FELIX-712 [4] boards are existing ATLAS components from the previous upgrade. The ALTI board is used to generate the clock, and the trigger signal while FELIX-712, a PCIe board, retransmits the TTC signal via the GBT protocol [7], receives data via the FULL Mode protocol [8] and sends them to its host computer workstation for storage. The mini-LATOURNETT is an Intel® cyclone®10 development kit implementation of the LATS (see Section 3.1), transmitting the configuration and pulse to the FEB2 and the CASAv2 boards. The CASAv2 board is a demonstrator of the calibration board (see Section 2.2), containing a LADOCv2B chip and a CLAROCv4B chip. It can generate a pulse in up to 4 calibration channels. The Detector emulator is a passive card that emulates the impedance of the real Liquid Argon Calorimeter detector. The FEB2v2.5 is a prototype FEB2 (see Section 2.1) containing ALFEv2 chips, COLUTAv4 chips, lpGBTv1 chips and VTRx chips. This board can read out 128 analog channels and send the digitised data for each bunch crossing over 22 optical links via the lpGBT protocol. The LASP-T2 is a LASP (see Section 3.2) Test board containing 2 Intel® Stratix®10 FPGA of two types (MX and SX). Only the MX FPGA is used on the readout. On this FPGA a simplified firmware is loaded that can receive, deserialise and align the data in time. Then, upon a trigger signal, it sends a configurable number of ADC samples to the FELIX acquisition system via the FULL Mode protocol.

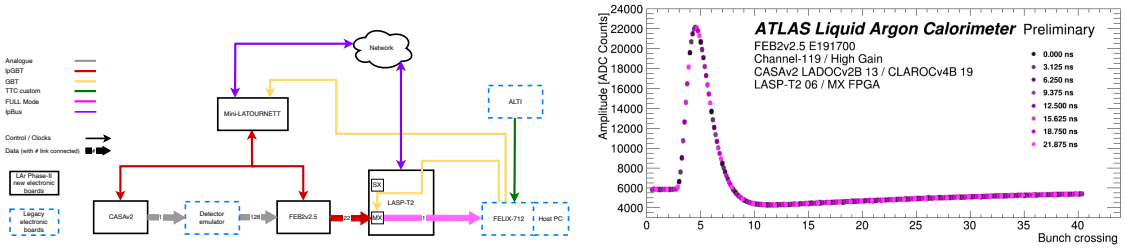

Figure 4: Technical schema of the CERN integration setup (left) used to record calibration pulses (right) [5].

The calibration pulse, generated and recorded on the setup described above, is presented in Figure 4. The trigger signals have been generated on a fixed BCID at a rate of 200 Hz. The LASP firmware is configured to send 40 ADC samples per trigger event. The pulse is generated by the CASAv2 with a constant amplitude. The pulse is then delayed by 1/8 of a bunch crossing by changing the position of the pulse command in the lpGBT frame between the mini-LATOURNETT

and the CASAv2. Each colour on the figure represents the samples recorded separately with one of the eight delay settings. The figure shows the recombination of the eight sequences, where the ADC sample position has been corrected to account for the timing shift. In total, 40 events per delay are overlaid. This integration setup is continuously evolving with the construction and inclusion of newer boards, and it is now beginning to incorporate hardware from other ATLAS subsystems.

The updated configuration is illustrated in the diagram in Figure 5. In this new setup, the ALTI system is replaced with the upgraded LTI system, which provides enhanced functionalities. This LTI protocol transmits additional information to the FELIX boards, including the trigger type, details about the BCID of the Level-0 Accept (L0A), and a dedicated user field that the LAr subsystem utilizes to propagate calibration pulses commands. To decode this upgraded signal, a new FELIX-182 card is used, replacing the previous FELIX-712 model for the LTI transmission. The FELIX-712 was kept for data recording. The LATOURNETT prototype, having successfully passed initial standalone tests, is now integrated into this setup, replacing the earlier mini-LATOURNETT version. Similarly, the CABANE board replaced the previous CASAv2 development board. This new setup is also integrating an upgrade version of the FEB2 (the v2.6 with minimal routing change with respect with the v2.5) and thanks to a splitter of the incoming data of one of the FEB2 data stream it is now similar to sending data equivalent to three FEB2 into one LASP FPGA allowing the test of the FW at such high data stream.

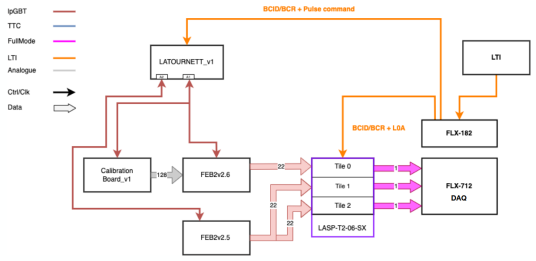

Figure 5: Technical schema of the ongoing setup with newer hardware.

This new integration environment is currently under active testing and will soon provide results, such as pulse measurement, using a configuration that more closely reflects the final hardware to be deployed as part of the ATLAS detector.

5. Conclusion

All the readout electronic of the ATLAS Liquid Argon (LAr) calorimeter must be upgraded before the start of the HL-LHC operation in 2030 to cope with the increased pile-up, higher radiation doses, and higher trigger rates. In particular, the on-detector electronics will now be capable of transmitting the full digitised signal to the off-detector at a rate of 40 MHz, enabling improvement in time and energy reconstruction computation method. Prototype boards have been successfully tested and are now being integrated to an increasingly more complete infrastructure, allowing for end-to-end readout tests using the upgraded hardware. The production of the on-detector ASICs has begun, and the mass production of all boards will start in the near future. Overall, the upgrade of the ATLAS LAr Calorimeter readout system is progressing according to schedule and remains on track for deployment ahead of HL-LHC operations.

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PoS(EPS-HEP2025)496