PROCEEDINGS OF SCIENCE

The commissioning and operational experience of the LHCb Upstream Tracker

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The LHCb detector has undergone a substantial upgrade, allowing the experiment to collect data with an all-software trigger, enabled by real-time front-end readout and rapid, efficient online reconstruction. The Upstream Tracker (UT), a four-plane silicon microstrip detector situated in front of the dipole magnet, is vital for reconstructing the paths of charged particles. The UT is crucial for tracking long-lived particles that decay outside the acceptance of the LHCb vertex detector, VELO. The UT was installed in LHCb in early 2023. The commissioning phase faced challenges due to data synchronisation issues associated with the read-out electronics. In this paper, we share lessons learned during the commissioning phase and operational experience from the first year of Run 3 data collection at LHCb, during which the performance of the UT was thoroughly examined.

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1. Detector Layout

The Upstream Tracker comprises 968 silicon sensors arranged across four detection planes and 68 vertical staves (figure 1), which contain a total of 536,756 strips [1]. There are four sensor types, each designed to meet different geometric requirements, including a circular cutout to fit the LHC beam pipe. The layout ensures extensive angular coverage and high granularity, which accounts for the expected particle flux in the detector. Each strip is readout by a SALT ASIC [2], a custom-designed chip with 128 channels and a six-bit amplitude resolution.

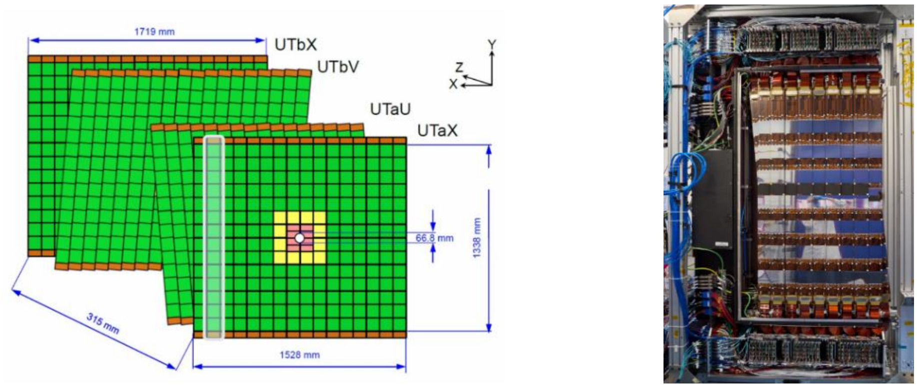

Figure 1: Schematic view of four UT layers (left). A UT half box in the open position (right) [1][3].

2. Commissioning of UT

The commissioning phase of the UT revealed several significant challenges. One issue was the instability of the clock signal delivered to the ASICs via the Time and Fast Control (TFC) system [4]. Certain Detector Control Boards (DCB) lose GBT–SOL40 [4] synchronisation (GBT - Gigabit Transceiver chip on the DCB, SOL40 - clock and control distribution board) under specific TFC sequences, causing ASIC misconfigurations and sometimes unrecoverable Forward Error Correction errors. The problem was addressed by implementing a strategy that ensured at least one bit of the TFC command remained asserted in each clock cycle, stabilising communication. Additionally, radiation-induced single-event upsets (SEUs) during collisions at the LHC caused occasional bit flips within the register bits of the ASICs. Such misconfigurations can degrade performance if left unaddressed (figure 2). A mitigation strategy was implemented at the detector control system level by frequently comparing and overwriting misconfigured registers with proper values.

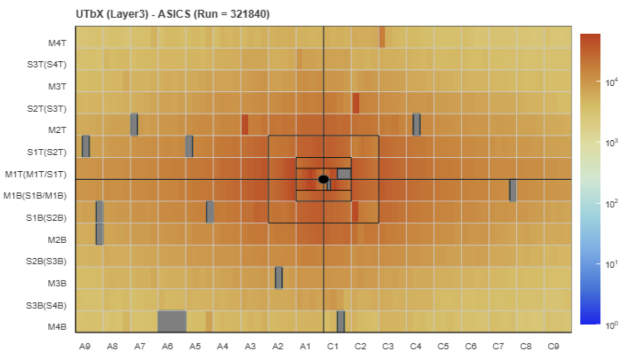

Figure 2: 2D map of signals recorded in 2025 versus simplified geometrical position for one UT layer. SEU-induced effects in several ASICs can be seen as hotspots in the distribution.

3. Calibration of UT

Precise calibration of the UT is essential for distinguishing particle signals from electronic noise. Calibration is performed using the dedicated VETRA software package [5], which executes an analysis over a series of electronic scans during beam-off periods. The calibration process included analogue baseline adjustments with an 8-bit trim DAC, digital pedestal corrections using a 6-bit register, determination of hit thresholds which distinguish electronic noise and particle signals, and identification of noisy or faulty channels. Figure 3 illustrates the sequence of front-end calibration steps, using data collected in the absence of LHCb collisions, on two representative UT hybrids. The top panel corresponds to a hybrid with a beampipe cutout, while the bottom panel shows an outer UT hybrid. The left column displays the channel readout after analogue baseline calibration. The middle column presents the corresponding readout following pedestal calibration and Mean Common Mode Subtraction (MCMS)[1]. The right column shows the RMS of the ADC signals as a function of channel number (blue line – before MCMS, red line – after). The reduced RMS observed in the top-right plot reflects the effect of the beampipe cutout.

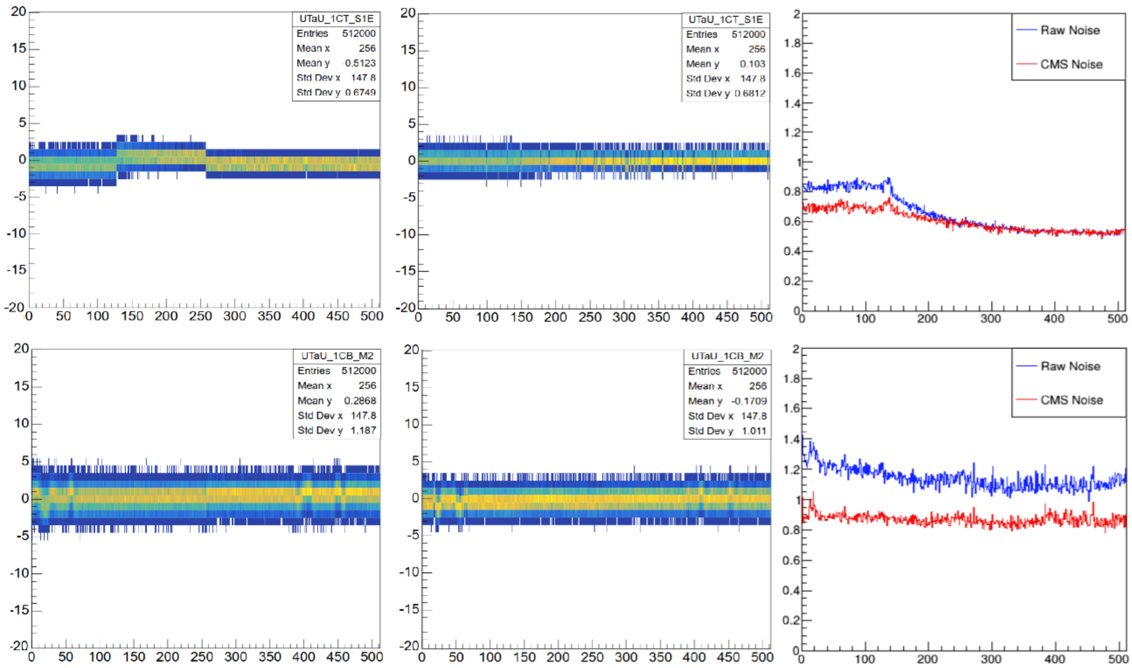

Figure 3: Frontend calibration steps for two UT hybrids: a hybrid with a beampipe cutout (top) and an outer hybrid (bottom). Shown are the channel readout after analogue baseline calibration (left), after pedestal calibration and MCMS (middle), and the RMS of ADC signals before and after MCMS (right). The reduced RMS in the top panel is due to the beampipe cutout.

4. Operation of UT

The performance of the UT was initially limited by bandwidth constraints of the readout board and by asymmetries in signal rates from specific ASICs, which caused data truncation through firmware protection mechanisms. To mitigate this, ADC thresholds were increased to suppress small signals and a limit on the maximum number of signals per ASIC was introduced

[1] Common Mode is the coherent, channel-to-channel correlated electronic noise shared by a front-end chip on a per–beam crossing basis; subtracting its mean suppresses this correlated noise and reduces the ADC RMS.

(figure 4 - top). Figure 4 – top left shows that higher thresholds were required in the central region; grey blocks indicate excluded or non-operational regions. Improvements in firmware design, together with reduced sensor noise from improved sensor cooling, resulted in a significant performance gain. After the updates, a more uniform threshold configuration across the detector became possible (figure 4 – top right). Figure 4 – bottom left illustrates the corresponding ASIC channel limits with the imposed restriction, while figure 4 – bottom right after improvements. The efficiency for reconstructing tracks with hits in both the Vertex detector (VELO) and the tracking stations (UT and SciFi [1]), requiring at least three UT hits, improved from 93.5% in 2024 to nearly 98.7% in 2025. Overall, 96.3% of active channels reflect the high operational readiness of the detector.

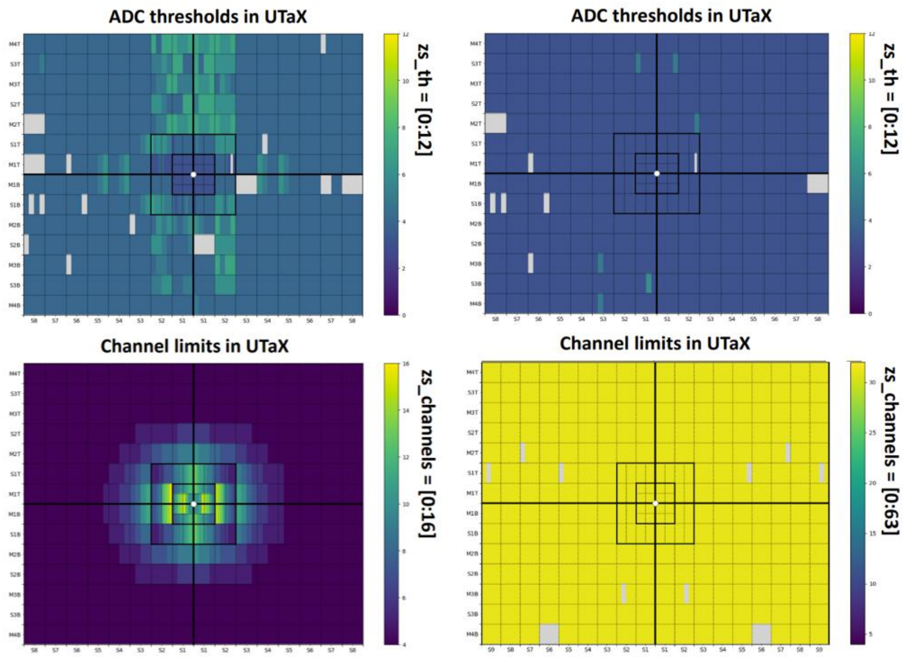

Figure 4: Top left: Simplified geometrical distribution of ADC hit thresholds for each ASIC on one of the UT layers, showing restrictions imposed on several ASICs before firmware improvements. Top right: Almost unrestricted thresholds after implementing firmware improvements. Bottom left: Simplified geometrical distribution of the maximum number of signals a specific ASIC could issue before firmware improvements, showing restrictions imposed on several ASICs. Bottom right: Unrestricted (63–by–chip design) maximum number of signals that a specific ASIC can issue after implementing firmware improvements.

5. Conclusions

The commissioning and operation of the LHCb Upstream Tracker involved overcoming significant technical challenges, ranging from unstable clock signals to environmental control and radiation effects. Through firmware development and systematic calibration, the detector has almost reached the designed levels of stability and efficiency. The experience highlights the importance of thorough early-stage testing, continuous firmware improvements, and meticulous calibration in achieving reliable long-term performance.

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