PROCEEDINGS OF SCIENCE

ATLAS ITk Pixel Detector Overview

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In the high-luminosity era of the Large Hadron Collider (HL-LHC), the instantaneous luminosity will reach unprecedented levels, with up to 200 proton-proton interactions per bunch crossing. To address the challenges posed by this environment, the ATLAS Inner Detector will be replaced with the all-silicon Inner Tracker (ITk). The innermost section of the ITk will feature a pixel detector comprising approximately 10,000 modules, covering a total active area of 13 m^2. To meet the evolving demands for radiation hardness, power dissipation, and production yield, the five barrel and endcap layers will incorporate several new technologies. The project is currently transitioning from pre-production to full-scale production, involving the fabrication of components, modules, mechanical structures, and services. This contribution provides an overview of the current status of the ITk pixel detector.

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1. The ATLAS experiment and the High-Luminosity LHC

The Large Hadron Collider (LHC) is the world's largest and most powerful particle collider. Located underground at CERN near Geneva, Switzerland, the LHC accererates two beams of protons and brings them to collision with a center of mass energy of 13.6 TeV at four points along the ring.

At one of these collision points, the ATLAS detector is situated to record the remnants of the proton-proton collisions. The ATLAS detector [1, 2] is a multipurpose particle detector with a forward–backward symmetric cylindrical geometry and a near 4π coverage in solid angle. It consists of an inner tracking detector surrounded by a thin superconducting solenoid providing a 2T axial magnetic field, electromagnetic and hadronic calorimeters, and a muon spectrometer. The inner tracking detector covers the pseudorapidity range $|\eta| < 2.5$. It consists of silicon pixel, silicon microstrip, and transition radiation tracking detectors. A two-level trigger system is used to select events [3] at an average of 100 kHz and 3 kHz, respectively.

The High-Luminosity LHC (HL-LHC) aims to increase the LHC's integrated luminosity by a factor of 10 beyond its original design value. This will be achieved through several technological upgrades, including more powerful focusing magnets and crab cavities that tilt the particle bunches prior to collision. The HL-LHC is projected to deliver 2500 fb^{-1} of data over 10 years, starting in 2030, with up to 200 proton-proton interactions per bunch crossing. This unprecedented dataset will enable precise measurements of Higgs boson properties, observations of rare Standard Model processes, and improved sensitivity in searches for new physics. Notable physics projections based on combined ATLAS and CMS datasets include a discovery significance of at least 4σ for Higgs boson pair production, an upper limit of 2.5% on the branching fraction of Higgs boson decays to invisible final states, and a 14% uncertainty on the measurement of $\sigma(t\bar{t}t\bar{t})$ [4].

2. The ATLAS ITk pixel detector

The success of the HL-LHC research program relies heavily on the performance of charged particle tracking. At the HL-LHC, the significantly higher particle density and increased radiation damage compared to current conditions will create a challenging environment for tracking. Additionally, the trigger rate is expected to increase from 100 kHz to 1 MHz, necessitating a higher data flow readout from the detectors. To meet these challenges, a new all-silicon tracking detector, the Inner Tracker (ITk), has been designed to replace the current ATLAS inner tracking detector. The ITk will consist of silicon pixel tracking layers surrounded by silicon strip tracking layers. Compared to the existing inner tracking detector, the ITk will feature higher granularity, a reduced material budget in the forward regions, enhanced radiation hardness, and extended tracking coverage up to $|\eta| = 4$.

A comparison of the ITk pixel detector with the current ATLAS pixel tracking detector is presented in Table 1. Compared to the current pixel detector, the ITk pixel detector will have more than five times as many modules, eight times the active area, and 55 times the number of readout channels. The ITk pixel detector will incorporate innovative design features and novel technologies to enhance tracking performance in the HL-LHC era, including thinner silicon sensors with smaller pixels, more radiation-hard readout chips, and a novel serial powering scheme.

Pixel detector	Current	ITk
Number of modules	1744	9164
Active area [m^2]	1.6	13
Number of channels	92M	5083M

Table 1: Comparison of the ITk pixel detector with the current ATLAS pixel detector.

2.1 Layout

The layout of the ITk Pixel detector is shown in Figure 1. The ITk Pixel detector will consist of five silicon tracking layers (L0-L4), divided into three distinct regions. The layout design balances tracking performance (hermeticity and material reduction) with detector buildability (cost and ease of construction). The detector consists of modules containing active sensor elements mounted onto lightweight carbon-fiber structures called *local supports*. The local supports also integrate cooling and services to power the modules and route the data.

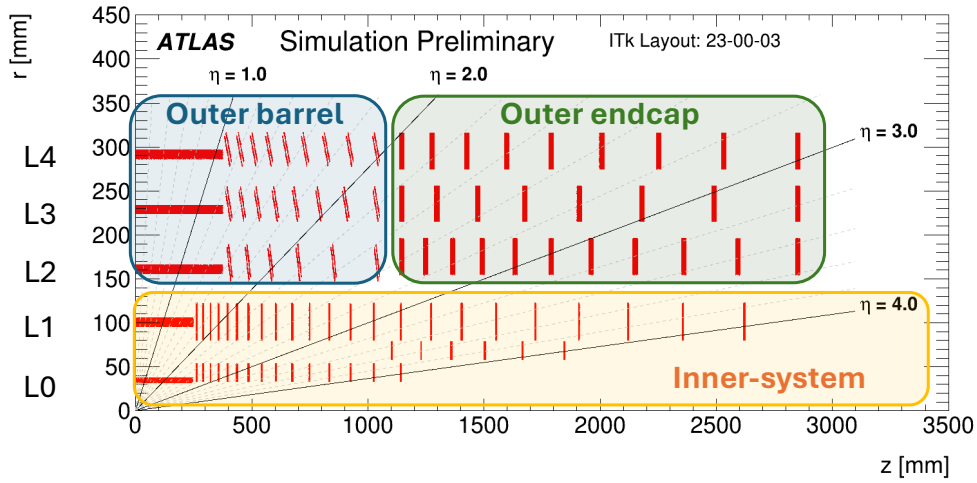


Figure 1: Layout of the ITk pixel detector in the r-z plane with different subsystems labeled [5].

The outer endcap region consists of outer endcap half-rings. A half-ring structure is chosen instead of the traditional disk structure to allow greater flexibility in sensor placement for optimal coverage while minimizing excess material. Additionally, the half-ring structure provides the benefit of routing services between adjacent half-rings.

The outer barrel region consists of longerons in the central area, surrounded by inclined half-rings in the outer regions. The active elements on these half-rings are tilted by 55°-67° with respect to the beam axis. This orientation improves tracking efficiency by aligning the sensors more perpendicular to the trajectories of charged particles originating from the interaction point. However, this configuration also increases the complexity of construction.

The inner system consists of a central region of staves and coupled-rings. The innermost two layers share a common support structure, which is designed to reduce material and service requirements in the most radiation-intense region. The entire inner system is independent of the

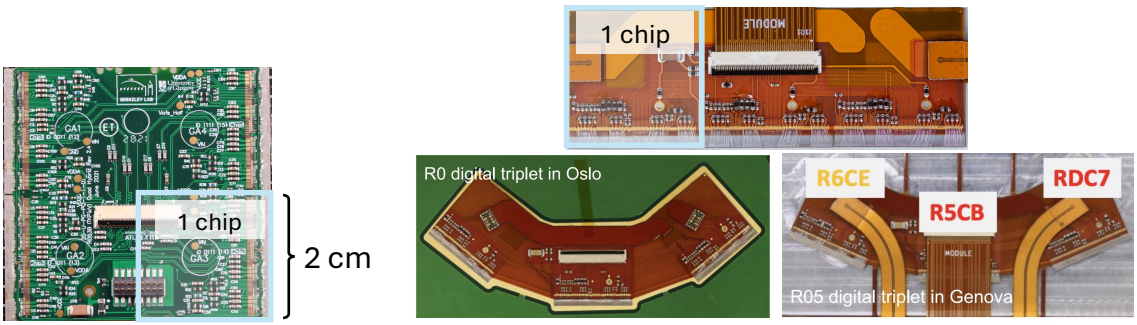
outer pixel regions, allowing for the possibility of replacement after reaching a critical radiation dose in the HL-LHC.

2.2 Pixel modules

The basic building block of the ITk is the pixel module. Pixel modules utilize hybrid pixel detector technology, where a passive silicon sensor is bump-bonded to readout chips. This allows for the separate optimization of sensor and readout chips, and can be produced with commercially-available technology. The readout chips are wire-bonded to a flexible PCB that is glued to the backside of the sensor. High-voltage (HV) reverse bias is applied to the backside of the sensor, creating a fully-depleted region inside of the silicon.

The detector is constructed primarily from a common module design, known as a quad module, which consists of a single 150 µm planar silicon sensor bump-bonded to four readout chips. A picture of a quad module is shown in Figure 2a. Each pixel measures $50 \times 50\,\mu\text{m}^2$. In the L1 barrel region, quad modules are built with 100 µm thick planar silicon sensors to enhance radiation hardness.

Triplet modules are used in the innermost layer in order to fit the detector geometry. Each triplet module, depicted in Figure 2b, consists of three 250 µm thick 3D silicon sensors bump-bonded to three readout chips. Compared to planar sensors, 3D silicon sensors exhibit higher radiation hardness, making them particularly suitable for the innermost regions of the detector. Triplet modules in the coupled-rings feature $50 \times 50\,\mu\text{m}^2$ pixels and are arranged in a ring formation with two different radii of curvature, depending on the ring. In the barrel region, triplet modules are arranged linearly and utilize $25 \times 100\,\mu\text{m}^2$ pixels to improve the resolution of track transverse impact parameters (d_0).



(a) Quad module **(b)** Triplet modules

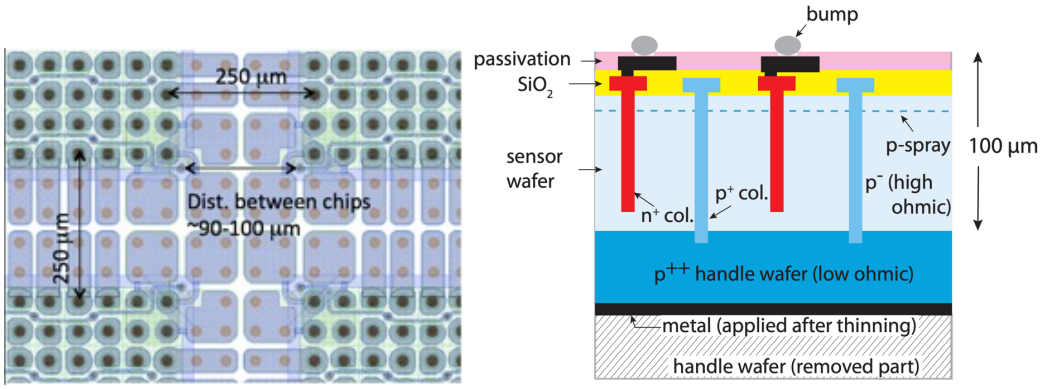
Figure 2: Modules used in the ITk Pixel Detector.

2.3 Sensors

Extensive R&D has been conducted to create silicon sensors capable of withstanding the intense radiation environment of the HL-LHC. Planar sensors utilizing n-in-p technology, in which n-type silicon is deposited on a p-type substrate, have been developed for quad modules [6]. These sensors are designed to be radiation-hard up to 4×10^{15} neq/cm^2 and can operate at bias voltages up to 600 V. Each pixel measures $50 \times 50\,\mu\text{m}^2$, except in the inter-chip region, where the pixel size is increased to avoid dead space between chips, as shown in Figure 3a. Compared to sensors in the

current inner detector, ITk pixel sensors are approximately 100-150 µm thinner and have four times smaller pixels [7].

The 3D sensors feature electrodes embedded as columns within the silicon bulk, as illustrated in Figure 3b [8]. These sensors are designed to withstand radiation levels up to 2×10^{16} n/cm^2 and require bias voltages up to 250 V. This technology has already been demonstrated in the ATLAS Insertable B-Layer and will be employed exclusively in the innermost ITk layer.



(a) **(b)**

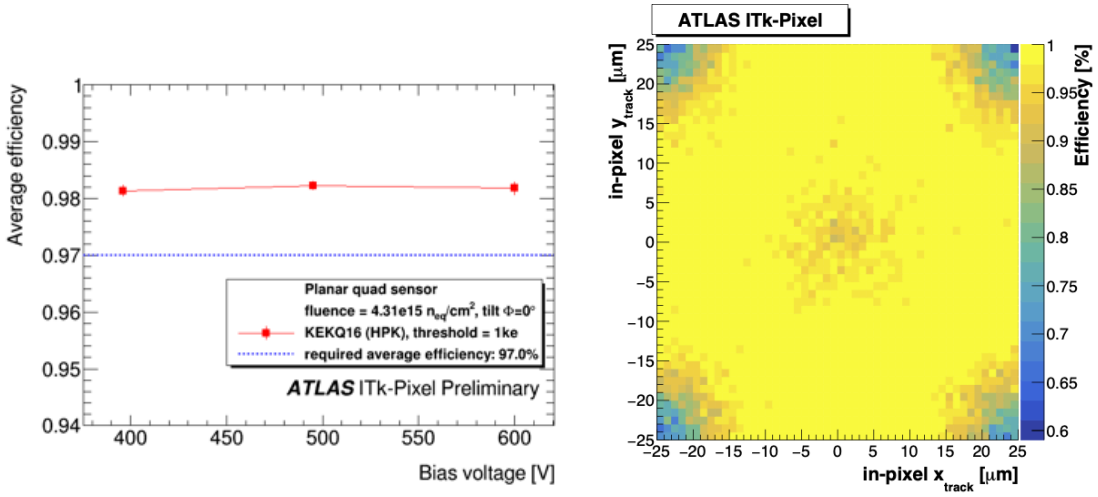
Figure 3: In (a), the larger pixels in the inter-chip region of a planar sensor on a quad module is shown. In (b), the electrode structure of 3D sensors is shown. Adaped from [9].

To test the performance of modules after irradiation, planar quad modules were irradiated up to 10^{15} n/cm^2, and 3D sensors bump-bonded to single readout chips (single-chip cards) were irradiated up to 10^{16} n/cm^2. These modules were subsequently tested at the CERN SPS test beam in September 2023. The irradiation results are presented in Figure 4. The average hit efficiency of the HPK planar quad module was measured at three different bias voltages. At all tested voltages, the efficiency exceeded the required threshold for ITk performance (97%). The average hit efficiency of the Sintef 3D single-chip card, shown in Figure 4b, was measured at 60 V bias for an irradiated sensor. The sensor demonstrated a high efficiency of approximately 100%, except in corner areas. These inefficiencies are attributed to the electrode columns and are expected in perpendicularly mounted 3D sensors. In the final detector, most tracks will intersect the sensor at an angle, increasing efficiency in the electrode regions. The slightly lower efficiency region (90%) in the center corresponds to the placement of the readout electrode within the pixel cells.

2.4 Readout chip

All modules in the ITk pixel detector are read out using the ITkPix front-end readout chip, developed over a period of ten years by the RD53 collaboration. Compared to current front-end readout chips, the ITkPix chip must meet stringent requirements [12], including:

- ~10 times higher radiation hardness,
- ~10 times larger effective trigger latency hit buffering (due to the ~4 times increased hit rate and ~2 times extended trigger latency),



(a) HPK planar quad module **(b)** Sintef 3D single-chip card

Figure 4: In (a), the average hit efficiency of an HPK planar quad module is shown as a function of the bias voltage applied to the module [10]. In (b), the average hit efficiency of a Sintef 3D single-chip card at different hit positions is shown [11].

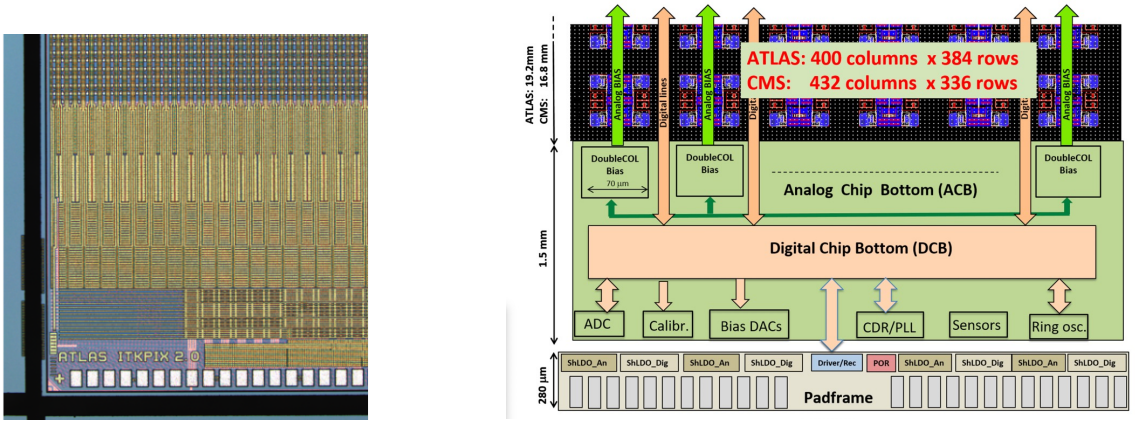
- ~100 times larger effective readout bandwidth (due to the increased trigger rate, higher hit rate, and smaller pixels)
- the same power consumption (< 1 W/cm^2)

The ITkPix readout chip, shown in Figure 5, is fabricated using 65 nm CMOS technology and is radiation-hard up to a total ionizing dose of 1 Grad. Each chip measures 2×2 cm and consists of 50×50 µm pixels, organized into 400 columns and 384 rows. When a pixel registers a charge exceeding the discriminator threshold, a 4-bit measurement of the time-over-threshold (ToT) is recorded. Unirradiated readout chips typically operate with a threshold of approximately 1000e-1500e and exhibit a noise level of ~40e.

A close-up image of one corner of the chip is shown in Figure 5a, while the overall chip floorplan is presented in Figure 5b. The chip consists of a pixel matrix and a control section at the bottom. The pixel matrix is constructed from identical 8×8 pixel cores, which are organized into columns. The lower section of the chip houses all system functionality, including wirebond pads for connectivity.

Currently, two versions of the chip are in use:

- **ITkPixv1.1**: A pre-production version used for module assembly, but not intended for the final detector. This version has a critical issue preventing ToT readout from the pixels and must therefore operate in binary readout mode.
- **ITkPixv2**: The production version with bug fixes and performance improvements, used for constructing detector-quality modules.



(a) **(b)**

Figure 5: In (a), a picture of one bottom corner of an ITkPix chip is shown, in which the pixel matrix, chip bottom, and bonding pads are visible. In (b), the physical implementation floorplan of the ITkPix chip is shown.

2.5 Serial powering

To minimize the material budget, a novel serial powering scheme is implemented for the first time in a large-scale detector [13]. ITkPix chips are equipped with Shunt Low Dropout (SLDO) power regulators, which dynamically adjust the shunt current to maintain constant local voltages on the chip. A simplified schematic of an SLDO element is shown in Figure 6a.

A conventional low dropout (LDO) regulator is used to power both the main load (L) and an internal load (L_s). The internal load (L_s) is actively controlled to satisfy the relation shown in Figure 6a, regardless of how much current the main load (the chip) draws. The offset voltage, V_0, and effective resistance, R_{eff}, are programmable parameters chosen to maximize efficiency while ensuring uniform current distribution among chips connected in parallel. The values are different for modules on different layers. The desired current-voltage relation for a chip with SLDO enabled is illustrated in Figure 6.

Each chip is equipped with separate analog and digital SLDO regulators, both connected in parallel to a common input power source. Up to 16 modules are powered in series with a constant current in a serial powering chain. Within each module, chips are powered in parallel to enhance the reliability of the serial powering chains, ensuring that individual chip failures do not affect other chips or modules in the same chain.

2.6 Data transmission and data merging

Reading out the data from a detector with more than 5 billion channels is a significant challenge. The readout dataflow is depicted in Figure 7. Data from each module is read out on up to 4 links per chip, each with a speed of 1.28 Gb/s. The data is routed to a patch-panel (PP0), and then through custom low-mass twinax cables (up to 6 m) to the optoboards. The optoboards aggregate the electrical links into high-speed optical links via the lpGPT chip. A common detector interface hardware, called FELIX [14], is used to read out the optical signal with 10.24 Gb/s fibres. To reduce material, links are shared at all stages.

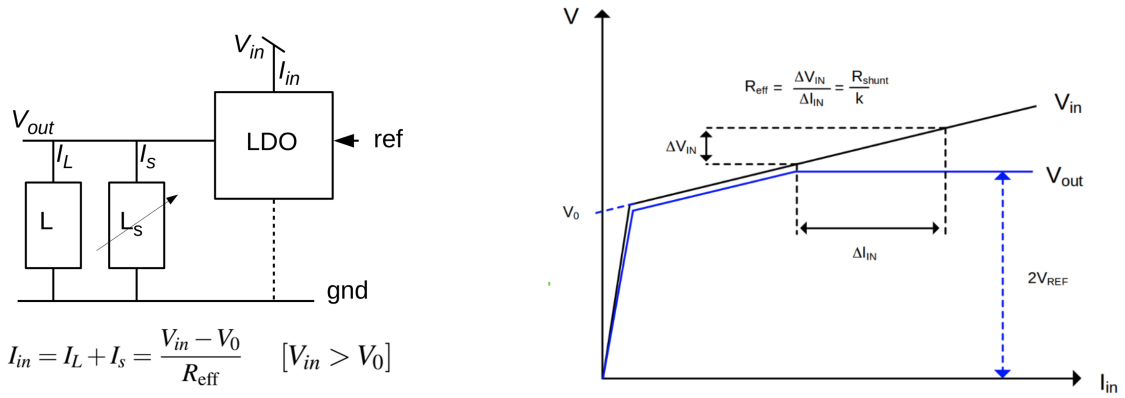


Figure 6: In (a), a diagram of a SLDO element is shown, which depicts the load current (I_L) and the regulated shunt current (I_s). In (b), the desired voltage vs. current relation for an SLDO element is shown.

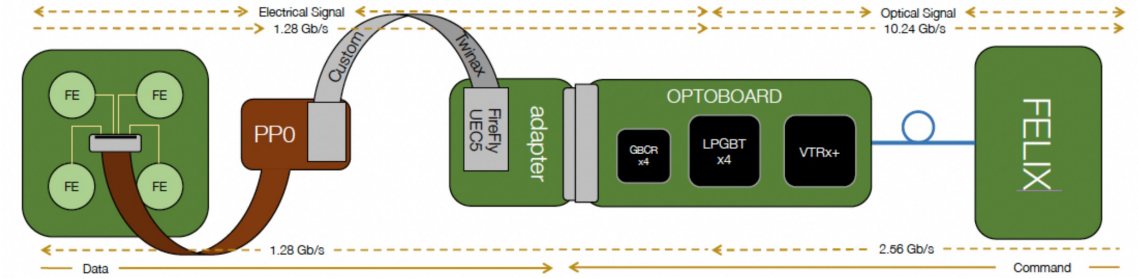
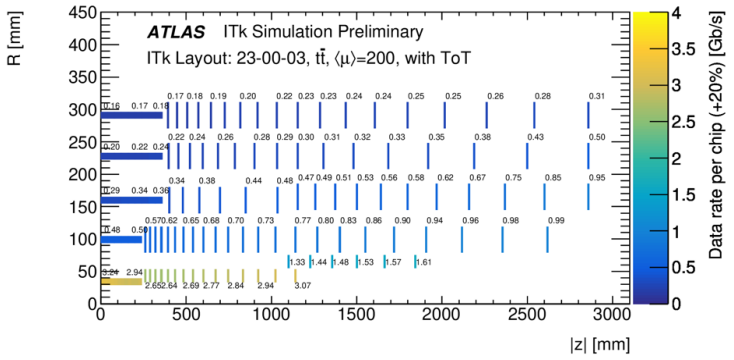


Figure 7: Schematic of the data transmission chaing for ITk Pixel modules.

The requirements on module design vary significantly depending on the position in the detector. The expected data rate for each tracking layer in the ITk Pixel detector with $\langle\mu\rangle = 200$ is shown in Figure 8a. The readout bandwidth varies from 4 Gb/s/chip in the innermost layer to 20-50 times lower in the outer regions of the detector. A key feature of the ITkPix chips is their high level of readout link modularity and flexibility, allowing for a common module design across the entirety of the detector. The link configurations for modules in different sections of the pixel detector are shown in Figure 8b. Each chip has up to four serial output links available, although only a single link is used if not all four are needed. While 4 links per chip are utilized in the innermost barrel region, the majority of the detector requires less than one link per chip. Therefore, the ITkPix chips have introduced the capability to merge multiple links. There are two merging configurations: In $2 \rightarrow 1$ merging, all data is read out from the module on two 1.28 Gb/s links (0.5 links per frontend). In $4 \rightarrow 1$ merging, all data is read out from the module on a single 1.28 Gb/s link (0.25 links per frontend).

2.7 Material budget

The ITk aims to achieve a reduced material budget, as this is important for tracking efficiency in a dense particle environment. To achieve this, the ITk detector has been designed with fewer cables using a serial powering scheme, thinner chips, low-mass support structures, and evaporative

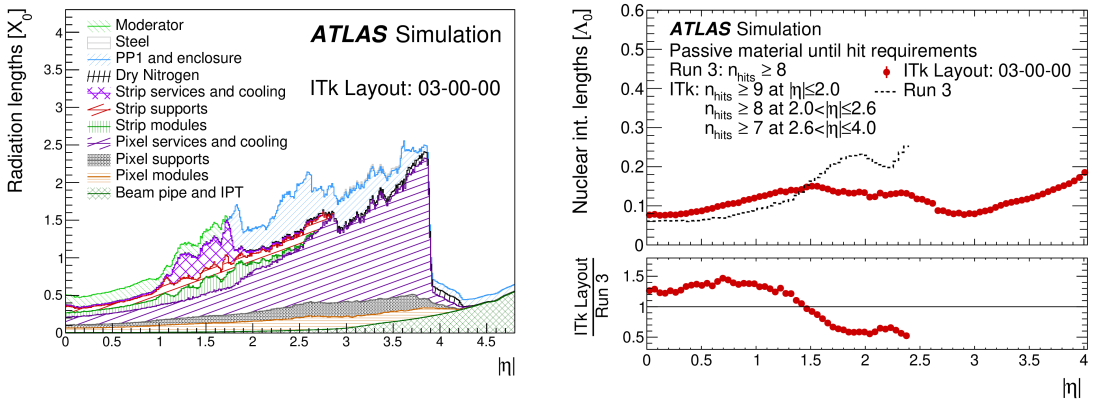


Layer	Section	Number of Links/FE
0	Flat barrel	4
	Barrel rings	3
	End-cap rings	2
1	Flat barrel	0.5
	Barrel rings	1
	End-cap rings	1
2	Flat barrel	0.5
	Barrel rings	0.5
	End-cap rings (1-5)	0.5
	End-cap rings (6-11)	1
3	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings	0.5
4	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings (1-7)	0.25
	End-cap rings (8-9)	0.5

(a) **(b)**

Figure 8: In (a), the estimated data rate in the ITk pixel detector is shown. The data rates include a 20% safety factor for all layers and sections. In (b), the number of links per front-end (FE) for the different regions of the pixel detector is shown. A fractional number of links / FE indicates that the link is shared between multiple chips [15].

CO_2 cooling with thin titanium pipes. The expected material distribution in the ITk detector is shown in Figure 9a. The largest component of the material budget comes from the pixel services (powering and readout) and pixel cooling. A comparison with the amount of material in the current ATLAS inner detector is shown in Figure 9b. Despite the aforementioned mitigations to reduce the material in the ITk, there is still an increase in the material budget in the central region ($|\eta| < 1.5$) of up to 50%, due to the much larger number of channels needing to be serviced and read out in the ITk detector compared to the current inner detector. There are significant reductions in material in the forward regions.



(a) **(b)**

Figure 9: In (a), the integrated radiation length traversed by a straight track as a function of the absolute pseuorapidity at the exit of the ITk volume is shown. In (b), a comparison of the material thickness in radiation lengths seen by particles until reaching the minimum number of hits required for track reconsturction in the ITk detector and the current inner detector is shown [16].

2.8 Expected tracking performance

A sample of $t\bar{t}$ events at $\sqrt{s}$ = 14 TeV is simulated in the ITk detector to assess the performance of the track reconstruction. The efficiency, shown in Figure 10, is defined as the fraction of charged particles with $p_T > 1$ GeV which are associated with a reconstructed track. The efficiency in the central region is expected to be maintained within 5% of the current inner detector, despite the larger material budget in that region. The efficiency in the forward region ($|\eta| > 2.5$) is similar to the one achieved in the central region.

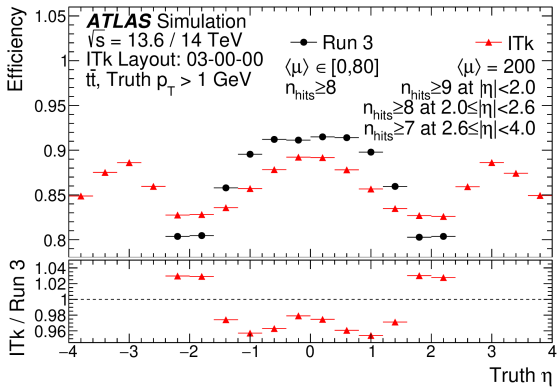


Figure 10: The expected physics tracking efficiency as a function of η in simulated $t\bar{t}$ events at $\langle\mu\rangle = 200$ for hard-scatter particles with $p_T > 1$ GeV with the ITk detector, compared to the current ATLAS inner detector with a uniform $\langle\mu\rangle$ distribution between 0 and 80 [16].

3. Module testing procedure and status

Approximately 12,000 pixel modules will be built for the ITk. Roughly 10% of these modules will be built in pre-production, for the purpose of validating the assembly, testing, and loading procedures. Module assembly begins with hybridization, in which the silicon sensors are bump-bonded to one or more readout chips. Flexible PCBs are then glued to the backside of the hybridized sensors and wirebonded to the readout chips. Modules are parylene coated to prevent HV discharge between the chip and the sensor. Roofs over the wirebonds are installed in outer-barrel modules to prevent damage during loading and installation. The modules then undergo a quality control (QC) testing procedure before being loaded onto local supports. Hybridisation takes place mostly at external vendors, while the remaining steps of module assembly are carried out at different ITk-institute labs.

3.1 Module quality control testing procedure

The module QC procedure aims to determine if each module will work in the ITk detector with the desired performance for the entirety of the HL-LHC. The QC procedure, as it is implemented for pre-production and early production, is described in the following section.

The QC procedure is divided into several testing stages, which are shown in Table 2. At each stage, either a full characterization of tests or a set of minimal tests are performed to ensure the

QC testing stages	Warm temp	Cold temp	Notes
Initial	✓	✓	Full characterization
Parylene masking	✓		Minimal tests
Post-parylene	✓	✓	Full characterization
Wirebond protection	✓		Outer-barrel modules only, minimal tests
Thermal cycing	✓		10× cycles between [−45°C, 55°C], 1× cycle between [−55°C, 60°C], minimal tests
Long-term stability test	✓		8 hours, minimal tests
Final	✓	✓	Full characterization

Table 2: Testing stages in module QC procedure.

Electrical test	Description
IV Scan	Scan bias voltage and measure leakage current through sensor
ADC Calibration	Calibrate internal analog-to-digital (ADC) converters
Analog readback	Check internal voltages and currents in chips
SLDO	Validate performance of Shunt Low-dropout (SLDO) circuits
VCAL calibration	Calibrate voltages used for charge injection
Injection capacitance	Measure capacitance used for charge injection
LP-mode	Validate chip operation in low-power mode
Data transmission	Check quality of data transmission
Minimum health test	Ensure performance of per-pixel digital and analog circuits
Tuning	Ensure ability to tune chips to desired threshold
Pixel failure analysis	Check quality of bump connection

Table 3: Electrical tests performed on a module for a full characterization in the QC procedure.

functionality of the module. Tests are performed at either room temperature (20 °C) or temperatures expected during operation (−15 °C for quad modules, −25 °C for triplet modules). The set of electrical tests performed in a full characterization are listed in Table 3. In addition to these electrical tests, several non-electrical tests are also performed in QC. These include metrology, a mass measurement, a flatness measurement of the backside of the module, and a visual inspection. Each test outlines a set of quality criteria that the module must pass in order to pass the QC test. The module passes a testing stage if it passes all tests at that stage. In total, there are approximately 45 electrical QC parameters and 20 non-electrical QC parameters in a full characterization. A full characterization of electrical tests on a single module takes about 1.5 hours.

Module assembly and testing is a global effort. Modules are assembled and tested at 25 different sites and loaded onto local supports at 9 different sites. All modules, however, will end up in the same detector and must be held to the same rigid standards. Ensuring consistency across testing stages and uniformity across testing sites is of utmost importance. For this reason, a common set of software tools is used to perform QC on the modules. These tools, collectively referred to as `Module-QC-tools`, are a set of Python packages that handle the collection of raw data from the

modules (including interfacing with lab equipment), the analysis of data and determination of the QC pass/fail flag, the data flow between the local testing labs and relevant databases, and the global analysis of module testing data.

In `Module-QC-tools`, raw module testing data is collected from modules and saved in the format of lightweight JSON files. Testing data is uploaded to the Local Database (`LocalDB`), which is the intermediate aggregation place of QC data that is local to each testing site. The `LocalDB` is a Python-Flask application that provides a web interface to assist ITk users in organizing both module QC measurements and detector control system information. Once all tests in a stage are complete, the user signs off the stage, and a summary of the testing results is uploaded to the production database (PDB), which is the global aggregation place of all data related to components and testing results of the ITk detector [17]. Communication with the PDB is performed with `ITkdb`, a Python wrapper around the PDB HTTP API. The common testing tools and data flow are designed to be flexible enough to allow for adaptations to the different testing setups adopted by each testing site, yet rigid enough to ensure that QC tests are always performed with the correct procedure.

3.1.1 Example: SLDO test

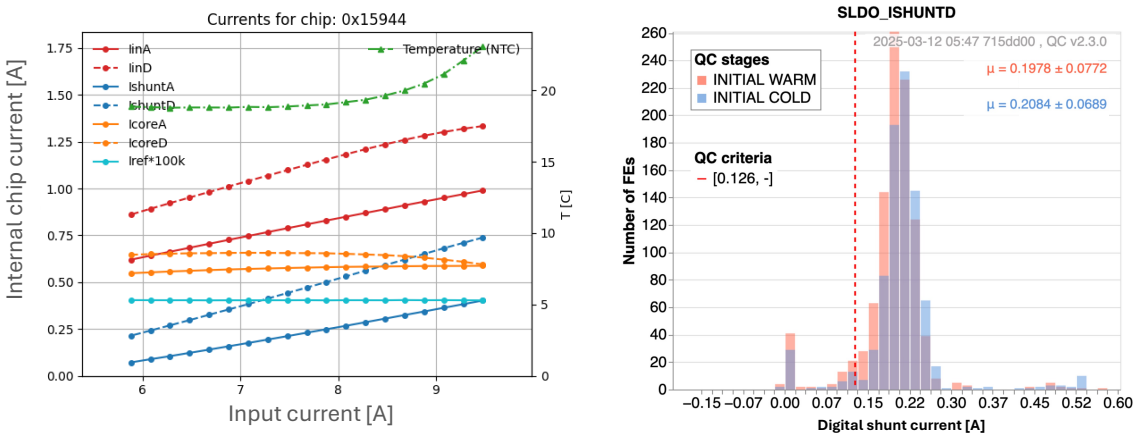
One of the most important tests performed in the QC procedure is the test of the module's SLDO powering performance. Testing the SLDO performance on the module is critical, as the effective resistance of chips on the same module can differ, preventing the current-sharing enabled by the SLDO elements from working as required. For this reason, the SLDO test is expected to be the module yield driver. In the SLDO test, the input current supplied to the module is increased beyond the nominal input current. At each input current tested, the chip's input, shunt, and reference currents, along with several of the chip's internal voltages, are monitored. If the SLDO is performing correctly, the shunt current should rise linearly with the module's input current, and the output voltage on the chip should remain constant, as described in Section 2.5. Furthermore, the chip's input voltage, input current, and shunt current for both the analog and digital parts are measured at the nominal input current and required to match the design expectations.

The results of an SLDO test for one ITkPixv1.1 readout chip are shown in Figure 11a. In this chip, the SLDO elements are behaving as expected for the majority of the input currents tested. There are some non-linearities that are especially apparent in the digital SLDO currents at high module input current.

The digital shunt current of all preproduction chips tested at the nominal operating current is shown in Figure 11b, at both the cold and warm initial testing stages. The majority of chips pass the QC selection, which requires that the activity-driven digital shunt current is large enough to ensure module operation in HL-LHC conditions. The peak at zero shunt current is due to chips with broken shunt elements or mis-measurements from early pre-production testing data.

3.2 Project status

An overview of the status of the ITk Pixel detector project is shown in Figure 12. Most parts of the project are moving from the pre-production to the production phase. In December 2024, the module assembly procedure passed the production readiness review, thus allowing for the start of production. The number of modules registered on the production database is shown in Figure 13.



(a) **(b)**

Figure 11: In (a), the internal chip currents as a function of module input current is shown for a quad module. The monitored chip currents include the input current (*Iin*), the shunt current (*Ishunt*), and the core current (*Icore*) for both the analog (*A*) and digital (*D*) parts of the chip, and the reference current (*Iref*). In (b), the digital shunt current measured at the nominal operating current for all pre-production readout chips tested is shown. The dashed red line indicates the lower selection on the digital shunt current in order for the readout chip to pass QC.

A marked increase in the rate of registered modules can be seen in early 2025, which reflects the start of production.

In the following year, the project will aim to increase the rate of module assembly by refining assembly procedures and streamlining the QC process. Assembled modules are now being used to load local supports in order to validate the loading procedures and prepare for the production of loaded local supports. Loaded local supports will be used for rigorous system tests, which will provide validation that the module QC procedure is effective at selecting modules that will work with the desired performance in the final detector.

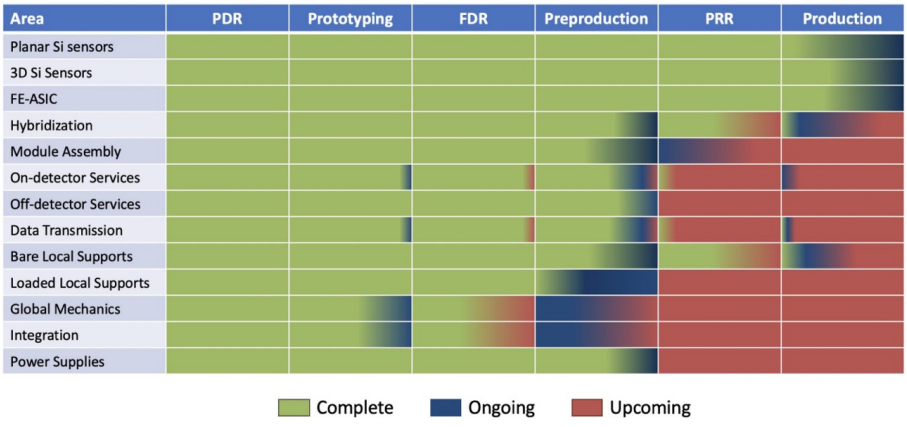


Figure 12: ITk Pixel project status as of November 2024. Columns indicate the current stage of each are, including whether the area has passed the preliminary design review (PDR), final design review (FDR) and production readiness review (PRR).

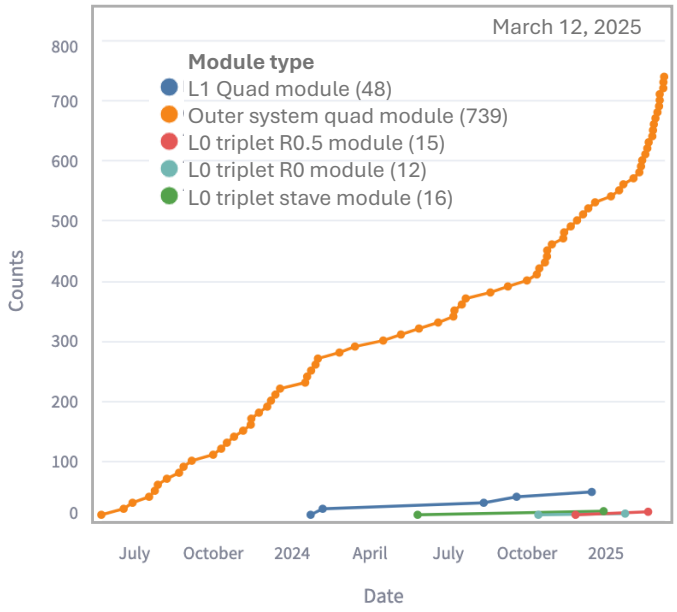


Figure 13: Number of modules (counts) registered on the production database as a function of time. The total number of each type of module registered as of March 2025 are indicated in parenthesis in the legend.

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