PROCEEDINGS OF SCIENCE

# Automated Testing Platform for LACT Electronics Board

**Zhanfei Mi,**[a] **Jinfan Chang,**[b] **Mingjie Yang,**[b,†,*] **Liangkun Zhang**[c,d] **and Aifeng Li**[a,†]

[a] *College of Information Science and Engineering/Shandong Agricultural University, Tai'an 271018, China,*

[b] *Key Laboratory of Particle Astrophysics Experimental Physics Division, Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China,*

[c] *University of Chinese Academy of Sciences, 19A Yuquan Road, Shijingshan District, 100049, Beijing, China*

[d] *Institute of High Energy Physics, Chinese Academy of Sciences, 19B Yuquan Road, Shijingshan District, 100049, Beijing, China*

*E-mail:* yangmingjie@ihep.ac.cn, liaf@sdau.edu.cn

The TIANFU Cosmic Ray Research Center, Chengdu, Sichuan, China plans to develop a Large Array of imaging atmospheric Cherenkov Telescopes (LACT). In the LACT project, the SiPM camera divides 1,616 pixels into 101 submodules to facilitate the development, testing, assembly, and maintenance of detector modules. Each module consists of a 4×4 pixel array and a 16-channel front-end electronics (FEE) board. The FEE board integrates two main functions: 1) It shapes and amplifies the analog pulses generated by the SiPM into narrow pulses, performs high and low-gain amplification, and subsequently digitizes them using an ASIC chip developed by IHEP; 2) It provides voltage-temperature compensation for the 16-channel SiPM under different temperature conditions. The LACT project requires 3,232 FEE boards. This study aims to develop an automated test platform to efficiently calibrate the analog pulse sampling and temperature compensation sections of the FEE boards.

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*Speaker





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# 1. Introduction

## 1.1 Large Array of imaging atmospheric Cherenkov Telescopes

The Large Array of imaging atmospheric Cherenkov Telescopes (LACT) employs a multi-telescope stereoscopic observation technique and a square-kilometer telescope array technology, significantly enhancing the sensitivity and angular resolution for detecting ultra-high-energy gamma-ray sources. It comprises 32 imaging atmospheric Cherenkov telescopes (IACTs) with 6-meter apertures. A structural schematic of a single telescope is shown in Figure 1. From top to bottom, it includes a Silicon Photomultiplier (SiPM) camera, a readout electronics system, a telescope support and rotation system, a reflector system, a slow control system, a power supply system, and a data acquisition system[1]. The Cherenkov light generated by charged particles produced during gamma-ray-induced atmospheric showers is collected and focused onto the SiPM camera by the reflector system for imaging. The SiPM converts the optical signal into an electrical signal, which is then measured by the backend electronics and converted into a digital signal. Finally, the data is transmitted via optical cables to the data acquisition center at the LHAASO[2] site.

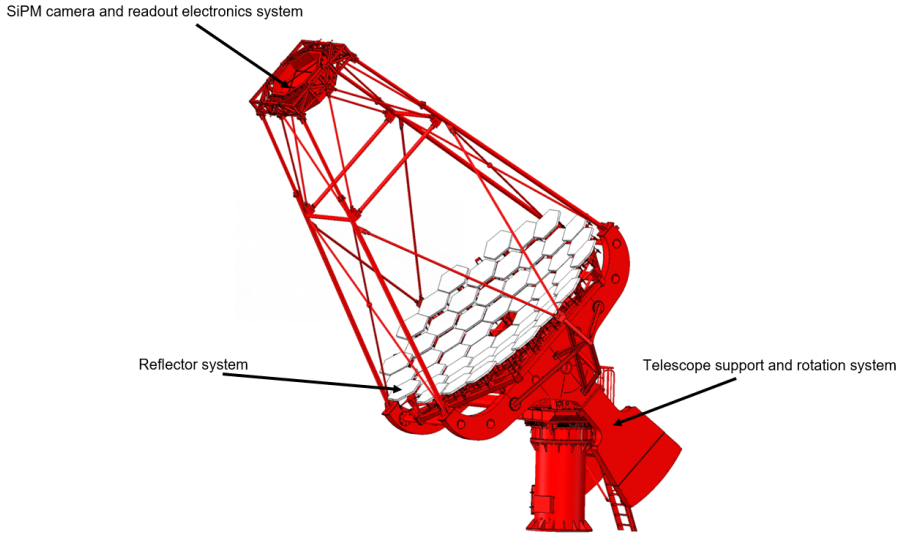


**Figure 1:** Telescope Structure Diagram

## 1.2 LACT Readout Electronics

The LACT readout electronics (FEE) board undertakes two core tasks: high-speed waveform digitization of silicon photomultiplier (SiPM) signals, and providing precise and stable operating voltage for the SiPMs. The waveform digitization solution employs the LACT-WAVE chip, a self-developed 16-channel switched capacitor array (SCA) chip with a 1 GHz sampling rate, designed by the Institute of High Energy Physics. This chip rapidly captures and stores analog voltages using 256 switched capacitor arrays, which are subsequently digitized and read out by downstream circuitry. Due to its unique structure, the chip requires precise calibration before use. In addition to high-speed sampling, each FEE board must supply independently adjustable operating voltages for 16 SiPM channels. Given the high-altitude location of the LACT project, significant temperature

variations can cause gain drift in SiPMs[3]. To maintain gain stability, the FEE dynamically adjusts the SiPM operating voltage via a DAC based on real-time temperature monitoring and employs an ADC for readback verification, thereby actively compensating for gain shifts induced by temperature changes[4]. The research presented in this paper covers both the calibration of the LACT-WAVE chip and the precise calibration of the SiPM operating voltage.

**Figure 2:** Physical Image of the FEE Board

## 2. Test Environment

### 2.1 Equipment Introduction

The TEKTRONIX AFG31000 is utilized as an external signal source, featuring real-time waveform monitoring, a large touchscreen interface, advanced waveform generation, and programming capabilities. It can be connected to a PC via Ethernet, enabling precise control over the output waveforms as required. The KEYSIGHT-34465A 6½-digit digital multimeter is employed to measure the voltage output from the FEE. It incorporates Truevolt technology for high-precision and stable measurements, and boasts a 4.3-inch color display for intuitive data visualization. Supporting a 1 A current range with pA resolution, it ensures accurate voltage and current measurements, automatically calibrates to compensate for temperature drift, and guarantees reliable performance throughout all-day testing. It comes standard with USB and LAN interfaces, with optional GPIB support for convenient connectivity to computers or other devices. The GWINSTEK GPD-4303S and KEYSIGHT E3633A are used to supply low voltage to the signal fan-out board and the FEE, while the GWINSTEK GPR-11H30D provides high voltage to the FEE.

## 3. FEE testing

### 3.1 High-Voltage Scaling and Calibration

Since SiPMs are highly sensitive to temperature, a high-voltage digital-to-analog converter (DAC) and high-voltage operational amplifier are integrated on the FEE to mitigate gain drift caused by operating in varying temperature environments. This enables the FEE to perform gain compensation for the SiPMs. In the PC-controlled scenario, the system employs the TCP communication protocol for bidirectional data exchange and circuit regulation: On one hand, the PC sends configuration commands via TCP to the high-voltage DAC in the compensation circuit, dynamically adjusting the output voltage parameters of the voltage regulation circuit. On the other hand, it simultaneously collects monitoring data from the ADC in the detection circuit in

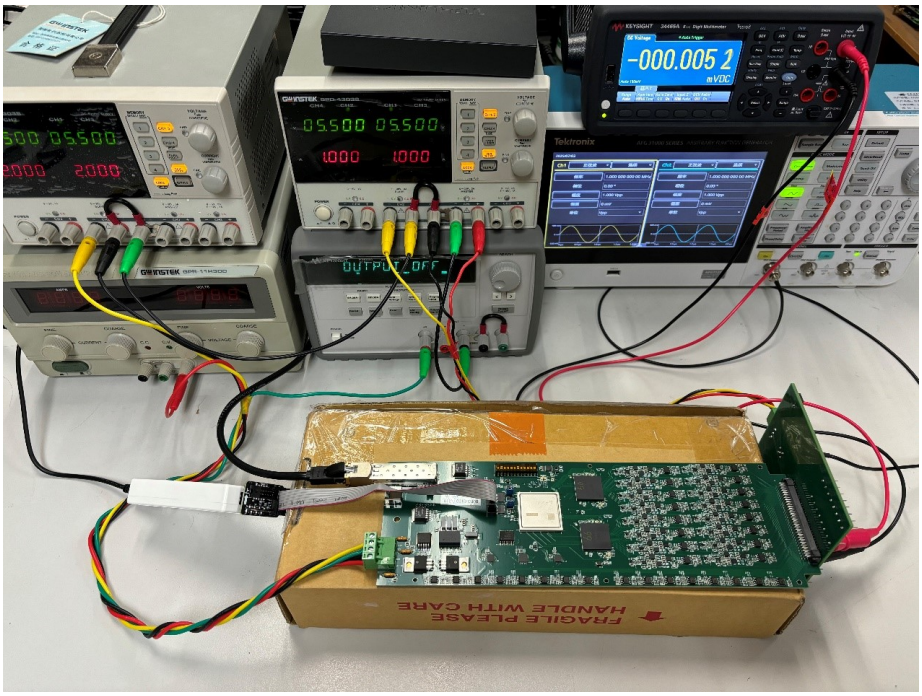


**Figure 3:** Test Environment Diagram

real time through TCP, achieving closed-loop monitoring of the circuit status. Meanwhile, the PC utilizes the NI-VISA instrument driver framework to send standardized read commands to a Keysight 34465A digital multimeter, accurately obtaining the actual output voltage value of the voltage regulation circuit. By comparing the theoretical output voltage derived from the high-voltage DAC configuration, the actual output voltage measured by the digital multimeter, and the voltage feedback from the ADC monitoring circuit, the system can simultaneously calibrate the output characteristics of the voltage regulation module and the linearity of the monitoring module. After linearity calibration, a set of linear parameters *k* and *b* is obtained. The distribution diagrams of the measured *k* and *b* values are shown in Figure 3. The upper two subplots display the distributions of the *k* and *b* values for the ADC, while the lower two subplots show the distributions of the *k* and *b* values for the DAC.

### 3.2 Scaling and Calibration of LACT-WAVE Waveform Sampling

The LACT-WAVE requires voltage calibration to correct the relationship between the ADC count values and the input voltage. For high-gain settings, a signal generator is used to input a direct current (DC) voltage ranging from 0 to 74 mV with a voltage adjustment step of 1 mV. The ADC count values corresponding to each DC input voltage are obtained by averaging the results of 256 samplings for the same DC voltage. For low-gain settings, a signal generator is used to input a DC voltage ranging from 0 to 1.8 V with a voltage step of 20 mV. Similarly, the ADC count values corresponding to each DC input voltage are obtained by averaging the results of 256 samplings for the same DC voltage. To eliminate errors caused by the sampling stop points, inaccurate sampling results before and after the sampling stop points were discarded. The voltage calibration results

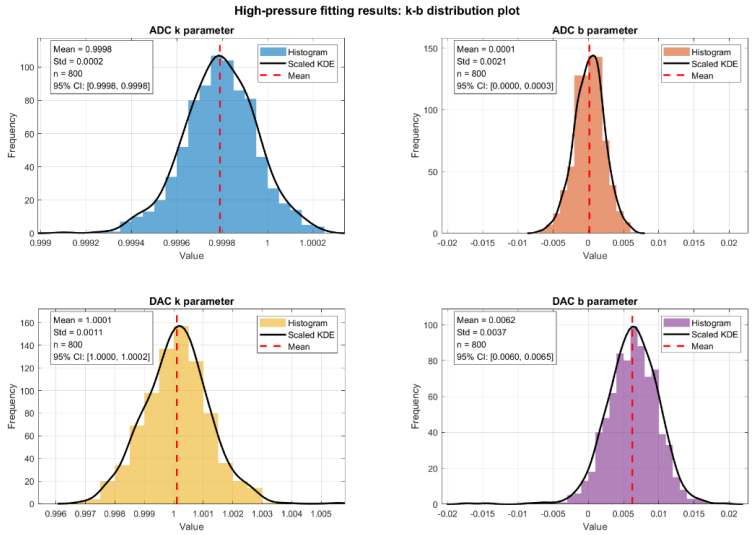


**Figure 4:** Distribution plot of FEE fitting results under high pressure

for the sampling channels of the high-gain and low-gain circuits of a single FEE board are shown in Figure 5 and7 . The voltage calibration results for the sampling channels of the high-gain and low-gain circuits of 100 FEE boards are shown in Figures 7 and 8.

## 4. Summary

This study developed an automated calibration system for the LACT project, designed to efficiently and accurately perform two core calibrations for the front-end electronics (FEE) boards: Firstly, based on TCP communication and NI-VISA control, the system calibrates the DAC/ADC modules using a high-precision multimeter, enabling closed-loop temperature compensation and linearity calibration (deriving parameters k and b) for the SiPM operating voltage. Secondly, voltage scaling is performed for the LACT-WAVE sampling chip by injecting precisely stepped DC signals and analyzing the response curves under high and low gain modes. The inherent measurement errors of its switched capacitor array are corrected through 256-sample averaging, thereby ensuring the accuracy and reliability of ultra-high-energy gamma-ray observation data.

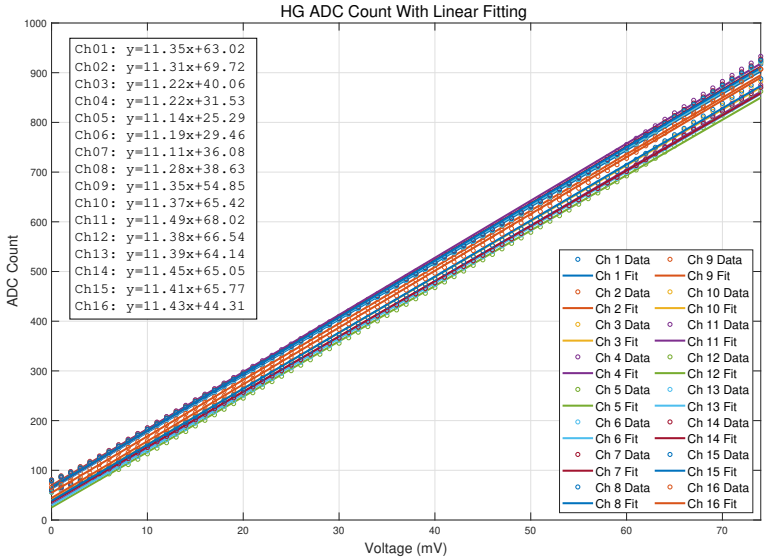


**Figure 5:** Voltage Scaling Results of Sampling Channels for High-Gain Circuits in a Single Front-End Electronics (FEE) Module

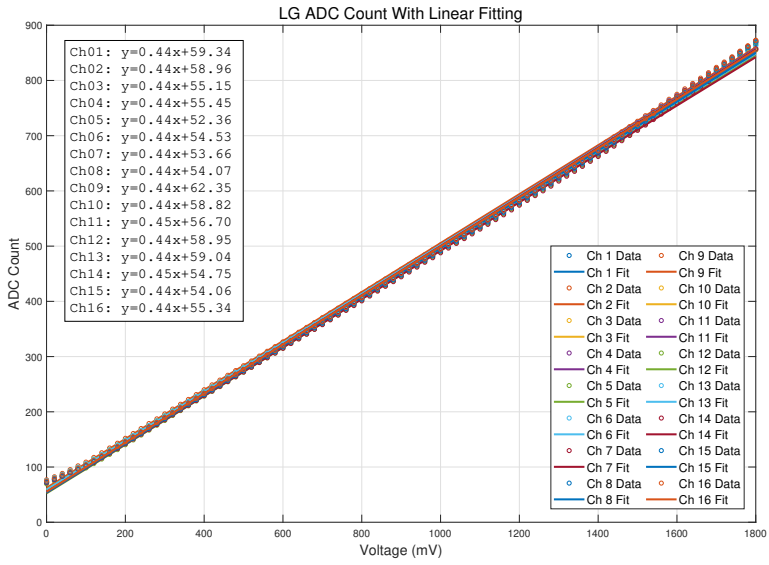


**Figure 6:** Voltage Scaling Results of Sampling Channels for Low-Gain Circuits in a Single Front-End Electronics (FEE) Module

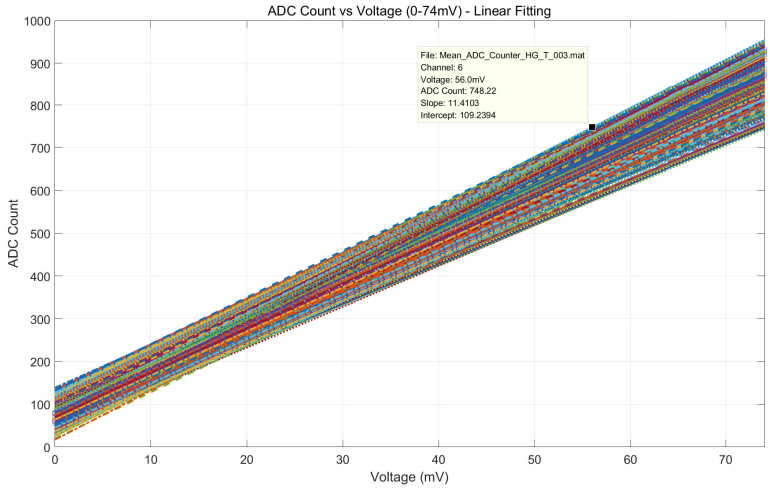


**Figure 7:** Calibration Results of Sampling for High-Gain Circuits in 100 Electronics Boards

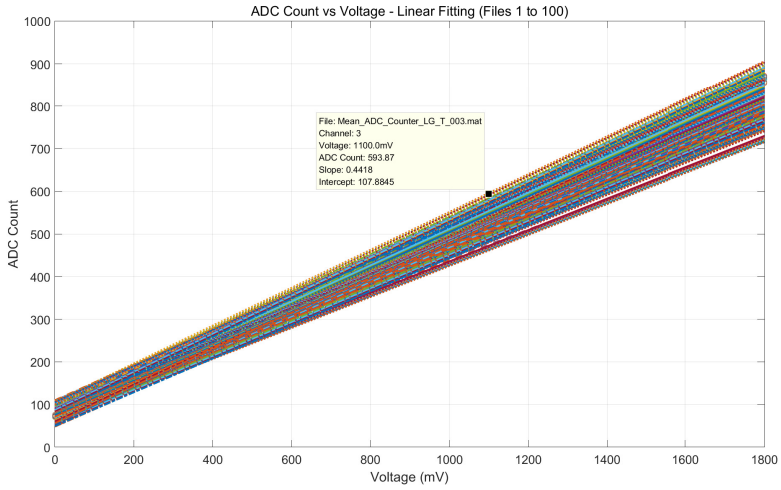


**Figure 8:** Calibration Results of Sampling for Low-Gain Circuits in 100 Electronics Boards

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