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ATLAS Inner Detector Operational experience at the Large Hadron Collider at CERN

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The tracking and vertexing performance of the ATLAS detector relies critically on the silicon and gaseous tracking subsystems that form the ATLAS Inner Detector. They have been successfully operated with high performance since Run 1 (2010) at the LHC. Those subsystems have undergone significant upgrades to meet the challenges imposed by the higher pileup and luminosity that are being delivered by the LHC, well beyond its original design goals. Furthermore, the Inner Detector was exposed to a radiation dose higher than has ever been experienced in any other detectors in high energy physics experiments. Effects of radiation damage on silicon sensors and front-end ASICs were intensively studied. The key status and performance metrics of the Pixel Detector and the Semi Conductor Tracker are summarised, and the operational experience and requirements to ensure optimum data quality and data taking efficiency are described.

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1. Introduction

The ATLAS experiment [1] is a general-purpose particle physics experiment designed to perform precise measurements of the Standard Model and to search for phenomena beyond the Standard Model using proton-proton and heavy-ion collision data provided by the Large Hadron Collider (LHC) [2] at CERN. The ATLAS detector consists of several subdetector systems arranged concentrically around the interaction point: the Inner Detector (ID) for charged-particle tracking, calorimeters for energy measurements, and the Muon Spectrometer. Since the start of LHC operations in 2010, ATLAS has collected collision data during Run 1 (2010–2011, $\sqrt{s}$ = 7 and 8 TeV), Run 2 (2015–2018, $\sqrt{s}$ = 13 TeV), and the ongoing Run 3 (2022–2026, $\sqrt{s}$ = 13.6 TeV). The LHC beam performance has steadily improved over the years through extensive upgrades and operational experience. During Run 3, the peak instantaneous luminosity has reached 2.2×10^{34} cm^{-2}s^{-1}, enabled by an increased number of protons per bunch thanks to injector upgrades and reduced emittance through the use of the BCMS filling scheme [3]. In addition, luminosity leveling and the accumulated operational experience allow the delivery of an excellent integrated luminosity, planned to reach more than 350 fb^{-1} over the five years of Run 3. These improvements in beam quality and delivered luminosity pose increasingly challenging conditions for the ATLAS detector, particularly for the innermost tracking system, the Inner Detector. This report focuses on the two silicon-based subdetectors of the ATLAS Inner Detector: the Pixel systems and the SCT.

2. ATLAS Inner Detector

The ATLAS Inner Detector (ID) consists of three subdetector systems arranged concentrically around the beam line: the Pixel Detector, the Semiconductor Tracker (SCT), and the Transition Radiation Tracker [1]. A 2 T axial magnetic field is applied within the ID volume, allowing the measurement of charged-particle momentum from the curvature of reconstructed trajectories, which are obtained by combining hits from the three subdetectors [4][5]. Primary vertices, corresponding to the proton–proton collision points, and secondary vertices, originating from heavy-flavor decays or long-lived hadrons, are reconstructed using these tracks.

The original Pixel Detector is based on n^+ in n planar silicon sensors with a thickness of 250 μm. It consists of three barrel layers and three endcap disks on each side, covering the pseudorapidity region up to $|\eta| < 2.5$, with radii between 50 mm and 150 mm from the beam line [6]. The barrel layers are denoted as the B-layer, Layer 1 and Layer 2, while the endcap disks are labeled Disk 1 to Disk 3. Each module has 46,080 pixels of mostly 50×400 μm^2, read out by 16 FE-I3 chips. One Module Controller Chip (MCC) per module serializes the raw data, including the time-over-threshold (ToT) information, and transmits it via two optical links (80 Mbit/s each) through the optoboard to the Pixel read-out driver (ROD) [7][8].

To mitigate radiation damage and maintain tracking and vertexing performance under high particle fluences, an additional barrel layer, the Insertable B-layer (IBL), was installed at a radius of 33.5 mm during the long shutdown between Run 1 and Run 2 [9]. The IBL was designed to cope with high hit occupancies and irradiation levels. It employs n^+ in n planar sensors of 200 μm thickness in the central region (75% of the modules), and n^+ in p 3D sensors of 230 μm thickness in the forward region (25% of the modules). The reduced pixel size of 50×250 μm^2 provides a finer granularity compared to the previous $50 \times 400\ \mu m^2$ pixels, improving tracking resolution and radiation tolerance. In addition, the new FE-I4 read-out chip is physically larger, covering a wider sensor area and allowing a simpler and more efficient module design without an MCC. In total, the Pixel system comprises about 92 million channels, including 12 million channels from the IBL.

The SCT is a silicon microstrip detector based on p in n sensors of 285 μm thickness [10]. It consists of four barrel layers and nine endcap disks on each side, covering up to $|\eta| < 2.5$, with radii from 250 mm to 550 mm [11][12]. The barrel layers are numbered Barrel 3 to Barrel 6, following the Pixel barrel numbering, while the endcap disks are labeled Disk 1 to Disk 9. Each silicon sensor has 770 strips, of which 768 are instrumented (bonded) with a readout pitch of 80 μm across a $6 \times 6\ cm^2$ active area. The majority of modules are formed by placing two pairs of the sensors ($6 \times 12\ cm^2$) back-to-back with a stereo angle of 40 mrad, allowing for two-dimensional hit position measurements. Signals are read out by six ABCD3TA chips per side, where they are amplified, shaped, and discriminated at a threshold of 1 fC [13]. The digitized signals are transmitted to the SCT ROD via two optical links per module with a full-speed bandwidth of 40 Mbit/s [14]. In total, the SCT comprises about 6.3 million read-out channels.

3. Pixel Detector operation and sensor performance during Run 3

The Pixel detector was operated successfully during LHC Run 1 and Run 2. In preparation for Run 3, several mitigation measures were implemented to cope with the higher occupancies resulting from improved beam quality, as well as to address hardware ageing and radiation effects.

During the long shutdown following Run 2, the optoboards were replaced to recover 30 modules that had failed data transmission due to the dead VCSEL channels. This hardware intervention restored full communication between the front-end electronics and the off-detector read-out system. In addition to these hardware recoveries, operational mitigations were introduced to ensure stable performance under Run 3 conditions. In 2024, six modules in Layer 1 were recovered by rerouting the data through a single optical link operating at half of the nominal readout speed, allowing continued operation with reduced bandwidth. Table 1 summarises the detector working fraction in 2018 (the last year of Run 2) and in 2024 and 2025 (the final two years of Run 3).

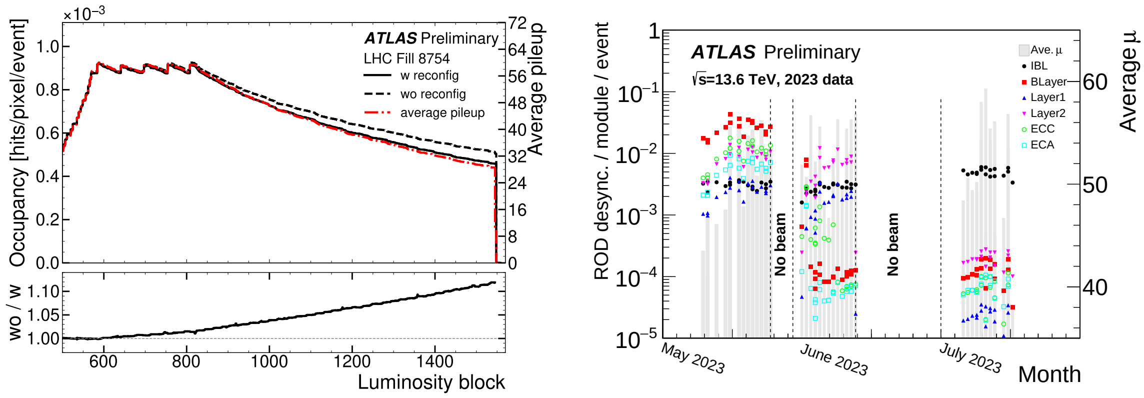
Table 1: Pixel and IBL detector working fraction over the years. The high working fraction is maintained through timely hardware interventions and optimisation of readout settings. The number of disabled modules is shown for the Pixel detector, while the number of front-ends is reported for the IBL.

Component	2018		2024		2025	
	Disabled/Total	Disabled [%]	Disabled/Total	Disabled [%]	Disabled/Total	Disabled [%]
Pixel B-Layer	18/286	6.2	21/286	7.3	22/286	7.7
Layer 1	29/494	5.8	18/494	3.6	19/494	3.8
Layer 2	33/676	4.8	50/676	7.4	61/676	9.0
Disk	15/288	5.2	16/288	5.2	15/288	5.2
Total (Pixel)	95/1744	5.4	105/1744	6.0	117/1744	6.7
IBL (FE)	3/448	0.7	5/448	1.1	5/448	1.1
Total (Pixel+IBL)	98/2192	4.5	110/2192	5.0	122/2192	5.6

High pile-up conditions lead to data corruption due to single event effects (SEE). During Run 2, the fraction of broken clusters caused by SEE reached up to 15% in the IBL [15].

To mitigate this, a front-end register reconfiguration procedure was introduced for Run 3. The procedure is executed every 5 seconds for a subset of modules in sequence. As a result, all front-end registers are refreshed once every 11 minutes. This operation is synchronised with the ATLAS global event counter reset and therefore introduces no dead time. Figure 1(a) shows the mean occupancy of IBL planar sensors and the pile-up during an LHC fill in 2023, with and without the reconfiguration. Without reconfiguration, the occupancy decreases more slowly than the pile-up due to noisy pixels, while with reconfiguration it follows the pile-up decay rate.

In addition to SEE, desynchronization between the module and the ATLAS central DAQ can occur when the data buffers of a module are fully occupied, leading to data loss for up to five seconds. To address this, a "Smart L1 forwarding logic" was deployed in the ROD firmware in 2023, which keeps track of the pending triggers for each module and stops forwarding triggers to single modules to avoid buffer overflow. Figure 1(b) shows the average ROD desynchronization per module per event before and after the introduction of the new logic in 2023. The introduction of the new logic significantly reduced the desynchronization rate for the Pixel detector.



(a) Occupancy and pile-up

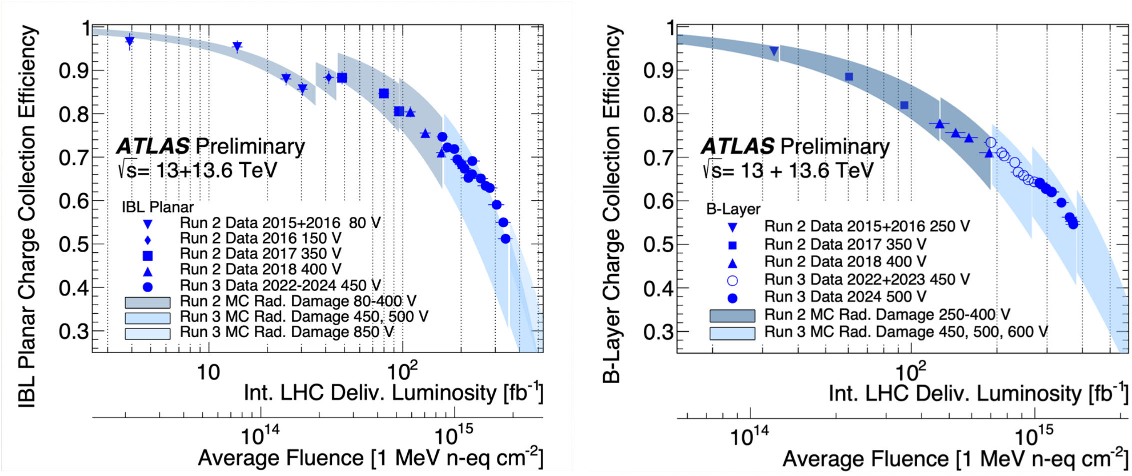
(b) ROD desynchronisation

Figure 1: (a) Mean occupancy of IBL planar modules and pile-up in a 2023 LHC fill with and without the reconfiguration. Source: ATLAS public plot "PIXE-2024-08, fig 01" [1]. (b) Average ROD desynchronization per module per event in 2023 data. Source: ATLAS public plot "PIX-2023-004, fig 01a" [2].

Radiation damage leads to a decrease in the charge collection efficiency (CCE), which is modeled with the new Pixel digitizer. The signal is simulated using electric field, Lorentz angle, and weighting potential maps, while accounting for carrier trapping and diffusion effects [16]. The simulated collected charge and CCE have been validated against data using the time-over-threshold (ToT) measurements from pp collisions. Figure 2 shows the CCE evolution for the most irradiated Pixel components, the IBL planar and b-layer sensors. Their CCE is expected to decrease to about 30% by the end of Run 3 in 2026, despite periodic adjustments of the bias voltage to maintain full depletion. Nevertheless, the hit-on-track efficiency remained around 98% in 2024 because the collected charge stayed well above the threshold, and this level of efficiency is expected to be maintained until 2026.

Similar studies have been performed for the IBL 3D sensors [17], which maintain higher CCE than planar sensors even at lower bias voltages.

[1] https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIXE-2024-08 (accessed 2025-10-06)
[2] https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2023-004 (accessed 2025-10-06)



(a) IBL planar **(b)** b-layer

Figure 2: Charge collection efficiency as a function of the integrated delivered luminosity and average fluence for (a) IBL planar sensors and (b) b-layer sensors, compared between data and ATLAS radiation damage simulation since the beginning of Run 2. Data points correspond to measurements, while the bands represent simulation predictions with their uncertainties. Increases in the bias voltage lead to the discontinuities observed in the curves. Source: ATLAS public plot "PIXE-2024-06" [3].

4. SCT operation experience and sensor performance during Run 3

The SCT has maintained a high detector working fraction and a hit detection efficiency of around 99% following its successful operation during LHC Run 1 and Run 2. Continuous replacement of off-detector hardware, such as DAQ and power-supply components, together with ongoing optimization of calibration software and operational parameters, has been essential to keeping the number of active strips high. Table 2 summarises the detector working fraction during Run 3, as derived from periodic calibration runs. Optical link redundancies that recover lost communication between the front-end and the ROD also help sustain the active strip fraction. The fourth and fifth rows in Table 2 list the number of modules using the trigger-transmitter and data-stream transmitter redundancies, respectively.

Table 2: Number of disabled components in the SCT and the corresponding active-strip fraction since the beginning of LHC Run 3. The top three rows list the disabled modules, chips, and strips. The fourth and fifth rows indicate modules using optical-transmitter redundancy. The last row gives the active-strip ratio relative to the total of 6.3 million strips in the SCT. Source: ATLAS public plot "SCTD-2025-02" [5]

Component	05/2022	12/2022	11/2023	12/2024	08/2025
Modules	46	47	49	51	57
Chips	85	81	88	171	183
Strips	24071	15310	15574	12738	13314
TX redundancy	58	59	50	51	53
RX redundancy	155	156	159	171	171
Active strips	98.3%	98.4%	98.4%	98.2%	98.0%

[3] https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIXE-2024-06 (accessed 2025-10-06)

The high pile-up conditions in Run 3 increase the data volume on the link between the front-end and the ROD (FE-links) and between the ROD and the ATLAS central DAQ (s-links). To cope with the higher occupancy, the DAQ system had already been expanded from 90 to 128 RODs before Run 2, providing sufficient capacity for operation in Run 3. In addition, the fibre remapping was performed to equalise the data load among RODs, successfully reducing failures due to DAQ backpressure. Together with the super-condensed readout mode introduced in Run 2, these updates ensured stable operation and excellent data quality in Run 3 [4]. Figure 3 shows the instantaneous luminosity, number of events, and the number of links with DAQ errors per event as a function of the luminosity block in a typical high pile-up run in 2024. The DAQ error rate, which mainly arises when the data volume exceeds the FE-link and s-link bandwidth, increases slightly under high pile-up conditions compared to Run 2, but has been kept below 0.5% of the total SCT channels.

The bias high-voltage (HV) required to achieve full depletion is monitored using two complementary measurements. HV scans are performed during pp physics runs to measure the hit-on-track efficiency as a function of HV. Figure 4 shows the HV scan results from Run 2 and Run 3. The HV required to maintain high efficiency increased after the type inversion of silicon sensor that occurred in 2017, but subsequently decreased due to beneficial annealing during the year-end technical stop. The operating HV is proactively raised each year based on the results of the HV scan.

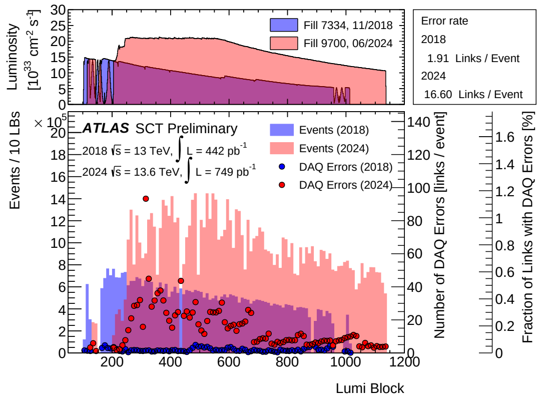


Figure 3: Instantaneous luminosity, number of events, and number of links with DAQ errors per event as a function of luminosity block, corresponding to operational time intervals of 60 s or less in pp physics runs during Run 2 and Run 3. The DAQ error fraction is shown together with the peak interactions per bunch crossing for a 2024 high pile-up run. Source: ATLAS public plot "SCTD-2025-02" [5]

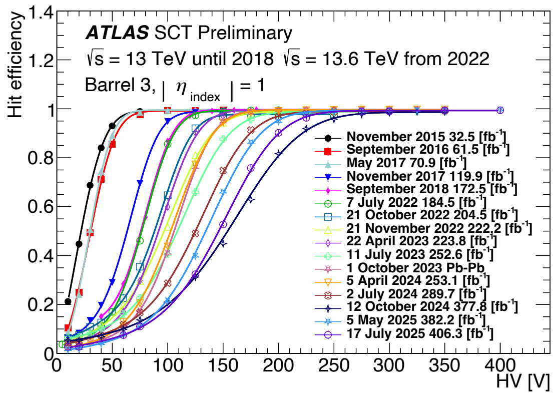


Figure 4: Hit efficiency as a function of the HV supplied to Barrel 3, measured using pp collision data from Run 2 and Run 3. The efficiency points are fitted with a skewed error function (solid lines), which empirically describes the observed trend. Source: ATLAS public plot "SCTD-2025-02" [5]

The full-depletion voltage is also evaluated from the HV dependence of the leakage current, measured in about six-hour calibration runs without beam, known as I–V scans. Figure 5 shows the evolution of the operating and supplied HV, leakage current and estimated full-depletion voltage since Run 1 for Barrel 3, together with the integrated luminosity and sensor temperature. The operating HV for Barrel 3 has been increased three times to match the rising full-depletion voltage, but a rapid increase in leakage current was observed in 2024. To mitigate this, the cooling-system

[4] https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/SCT-2017-002/ (accessed 2025-10-06)

temperature setting for Barrel 3 was lowered by 7 °C, effectively reducing the sensor temperature and stabilizing the HV current within power supply limits (5mA) until 2026. The large drop in HV current observed at the end of 2024 in Fig. 5 corresponds to this temperature change, and the measured leakage current agrees well with the Hamburg-model prediction even after the adjustment.

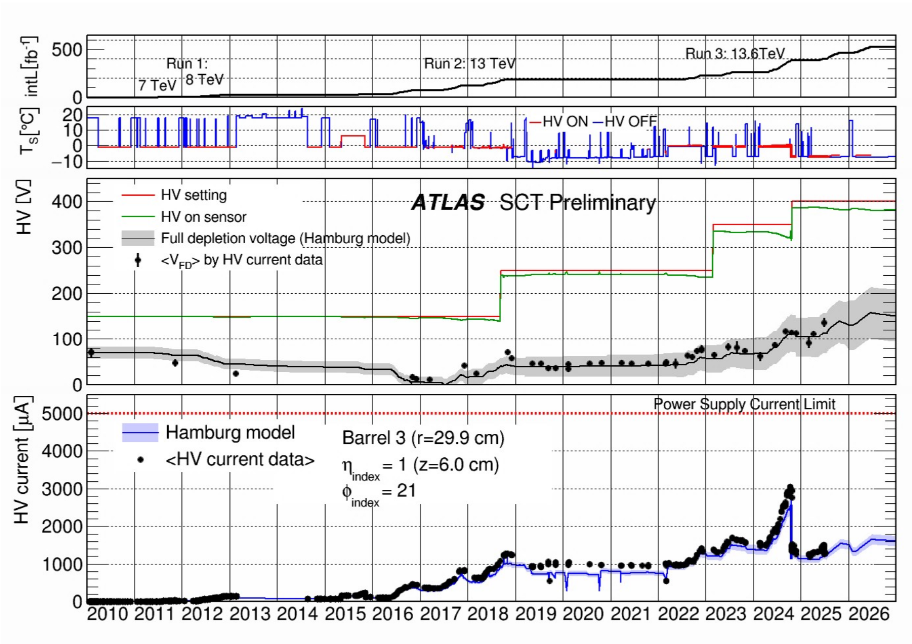


Figure 5: Evolution of the module high voltage (HV) for central Barrel 3 modules from 2010 to the end of 2026. From top to bottom: (1) integrated luminosity, (2) sensor temperature (with the red line indicating the expected temperature rise due to bulk heating from leakage current), (3) HV setting (red), actual HV on the sensor (green), and full-depletion voltage estimated by the Hamburg model (black, with points from I–V scans), and (4) evolution of leakage current from data (points) and Hamburg-model predictions (blue line). Source: ATLAS public plot “SCTD-2025-02” [5]

5. Summary

The high performance of LHC Run 3 is challenging for the ATLAS Inner Detector in terms of the DAQ performance and the high radiation levels. However, Pixel and SCT in the ATLAS Inner Detector have delivered excellent performance in LHC Run 3 by the continual improvement in the firmware, the optimization of the operational parameters and the accumulated experience of the operations The simulations and predictions of key parameters, such as the CCE and the full-depletion voltage, show good agreement with the data, suggesting that optimal performance will be maintained until the end of LHC Run 3.

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[5] https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/SCTD-2025-02/ (accessed 2025-10-17)

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