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ALICE ITS3 MOSAIX stitched wafer-scale sensor – Implementation challenges and solutions

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MOSAIX is a full-scale, full-size monolithic CMOS pixel sensor prototype developed for the ALICE Inner Tracking System 3 (ITS3), which will replace the three innermost layers of the ALICE tracker during the LHC Long Shutdown 3 (LS3). With over 26 cm in length and 2 cm in width, MOSAIX contains 12 Repeated Sensor Units (RSUs). A single RSU has 12 pixel matrix tiles, each with 444×156 pixels and a pixel dimension of $22.8 \times 20.8\,\mu\text{m}^2$. Power supply and data lines of each RSU are connected by stitching to the power pads on the Left and Right Endcaps and to the readout processing block in the Left Endcap, respectively. MOSAIX is designed to operate with air cooling only and redefines the limits of monolithic CMOS pixel detectors, spanning an entire wafer while pixels maintain over 99 % detection efficiency and a fake hit rate below $0.1\,\text{pixel}^{-1}\,\text{s}^{-1}$. By thinning MOSAIX to 50 μm and supporting it only with ultra-light carbon-foam structures, the ITS3 achieves an average material budget of 0.09 % X_0 per layer. Developing an ASIC of this size introduces challenges that go beyond traditional design boundaries. Wafer production failures, no longer confined to individual dies, must be considered by design across the entire stitched wafer. The architecture addresses this by implementing the sensor as a distributed system, where repeated processing units are integrated into a continuous structure and maintained through localized control and fault isolation. With all power and data I/O connections constrained to the short edges, the system must sustain over 30 Gb/s of throughput while remaining below $40\,\text{mW/cm}^2$ power consumption. This contribution will show how architecture, yield resilience, and power distribution management converge in MOSAIX, illustrating the design principles behind one of the most ambitious wafer-scale detectors built to date.

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1. Towards the ITS3 Upgrade

The Inner Tracking System 3 (ITS3) of the ALICE experiment [1] is conceived as a fully cylindrical, self-supporting vertex detector based on wafer-scale monolithic pixel sensors. This new design removes the need for mechanical staves and associated cooling structures, leading to an exceptionally low material budget of 0.09 % X_0 per layer. The detector will rely on air cooling only, imposing a strict constraint on the power budget of the sensors. In comparison with the stave-based ITS2, where the sensors were mounted on flexible printed circuits with liquid cooling and a per-layer material budget of roughly 0.36 % X_0, the ITS3 architecture, illustrated in Fig. 1, provides a substantial reduction of passive material and a corresponding improvement in tracking precision and impact-parameter resolution close to the interaction point.

Achieving such a detector concept poses several challenges for the sensor design. The architecture must integrate data aggregation and transmission, previously handled via staves and flexible printed circuits, directly on-chip. It must ensure uniform power distribution over the wafer-scale stitched area, support high-speed serial links with a total bandwidth of 30.72 Gb/s, maintain high yield despite the large area, and operate at a power density below 40 mW/cm^2. To address these requirements, MOSAIX has been developed as a full-size, fully functional prototype for the ITS3 upgrade, implemented in TPSCo 65 nm CMOS technology.

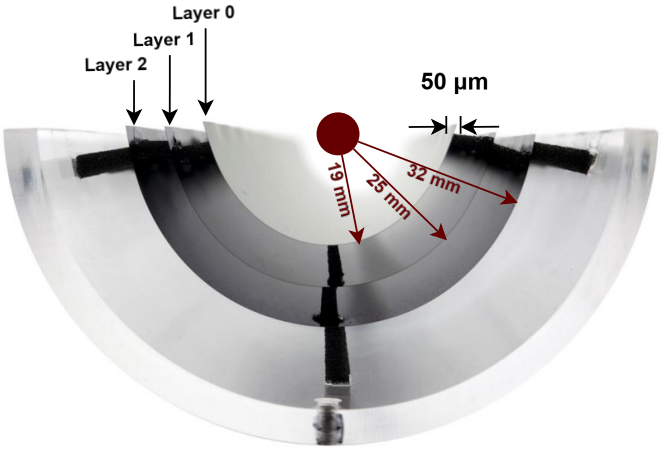

Figure 1: Mechanical model of the ITS3 half-barrel.

2. Architecture of MOSAIX

In standard semiconductor manufacturing, the reticle field of a lithography system is limited to a few square centimeters, which constrains the maximum chip size. However, certain CMOS imaging technologies support stitching, where adjacent reticle exposures are precisely aligned to form a continuous pattern across the wafer. This technique enables the production of large-area circuits that exceed a single reticle field. In this case, a reticle layout contains all building blocks of the design and is repeatedly exposed across the wafer with precise alignment between stitching boundaries. MOSAIX building blocks stitched together form an independent, fully functional sensor referred to as a segment, as shown in Fig. 2. Depending on the radii of the target ITS3 layer, the wafer is diced into up to six stitched segments [2]. This modular layout allows a single design to serve all three cylindrical layers of the ITS3 detector.

As depicted in the Figure 3, MOSAIX is built by three building blocks: the Repeated Sensor Unit (RSU), repeated twelve times, and two edge blocks, the Left Endcap (LEC) and the Right Endcap (REC). The Endcaps

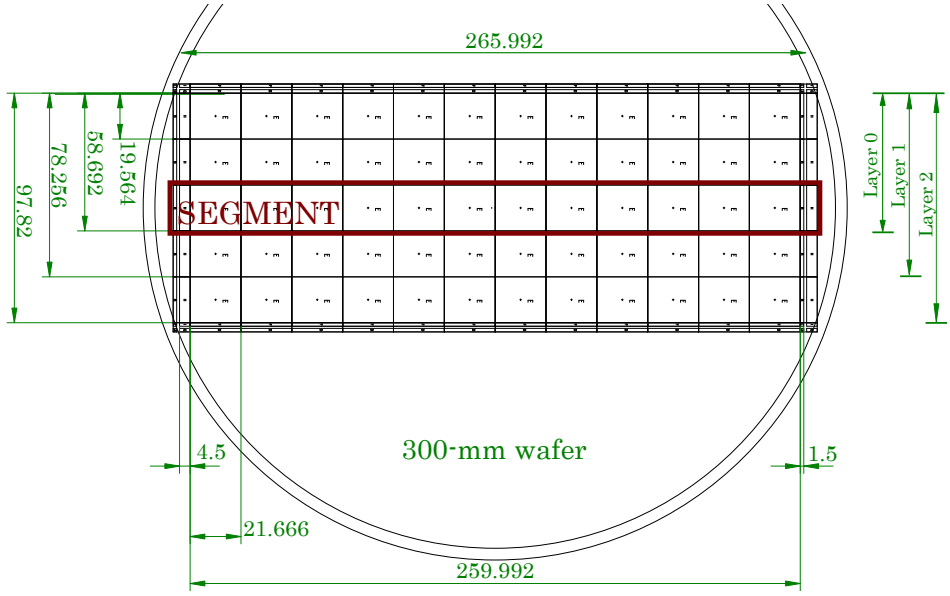

Figure 2: MOSAIX wafer map.

provide all external interfaces to the detector system. Power is supplied from both edges of the wafer, while clock, reset, and control signals originate in the LEC and are distributed across the wafer to all RSUs. Data generated within the RSUs propagate from right to left, being aggregated in the LEC, which performs the final serialization and transmission off-chip. The LEC integrates eight 10.24 Gb/s serializers with lpGBT [3] frame encoding. Each RSU contains approximately 0.8 M pixels and operates as an independent functional block.

2.1 Repeated Sensor Unit

The RSU is divided into two halves mirrored along the horizontal axis and assembled by repeating smaller building units, making the design as modular as possible. The overall architecture is shown in Fig. 3, which is not to scale. The achieved sensitive area is 93% of the total RSU area. Each RSU is further composed of twelve Tiles, a Stitched Backbone (SBB) for on-chip data and clock transmission over the large area, and a Service Node (SRV). SBB and SRV are repeated every three tiles. Tile is the fundamental building block of MOSAIX. It consists of four sub-blocks: the Unit Bias, the Pixel Matrix, the Periphery, and Power switches that allow each Tile to be powered on or off independently. Each Tile can also be independently biased and read out, while sharing global clock, reset, and sync signals. There are in total 144 Tiles per segment. The Unit Bias block includes six on-chip DACs that provide bias voltages for the pixel analog front-end. The pixel matrix contains 444×156 pixels with a pitch of $22.8 \times 20.8\,\mu\text{m}^2$. Each pixel has an analog front-end (FE) and a digital part with two memory registers for hit storage. The front-end is designed for a detection efficiency above 99% for particle rates up to $4.4\,\text{MHz/cm}^2$ and a fake-hit rate below $0.1\,\text{pixel}^{-1}\,\text{s}^{-1}$. MOSAIX includes twelve pixel variants based on the MOSS [4] front-end circuitry, combining six front-end and two bias-block configurations. One segment contains 144 matrices, corresponding to 9.97 Mpixels in total. Periphery reads and processes data from the matrix and sends them to the Stitched Backbone (SBB). Figure 4 depicts the high-level data flow inside the Periphery. It includes four Readout Region Units (RRUs) operating in continuous mode. Data are stored in parallel in four dedicated FIFOs. Data processing is handled by the Top Readout Unit (TRU) state machine, which transfers the data to the serializer. The serializer operates at 160 MHz, while the rest of the logic runs at 40 MHz. The serializer output is sent to a differential transmitter (Tx) that interfaces with the

SBB. This interface is implemented as a dedicated analog IP integrated within the digital-on-top Periphery. A physics-driven data model was used to parametrise the Periphery and find an optimal configuration, as described in [5] .

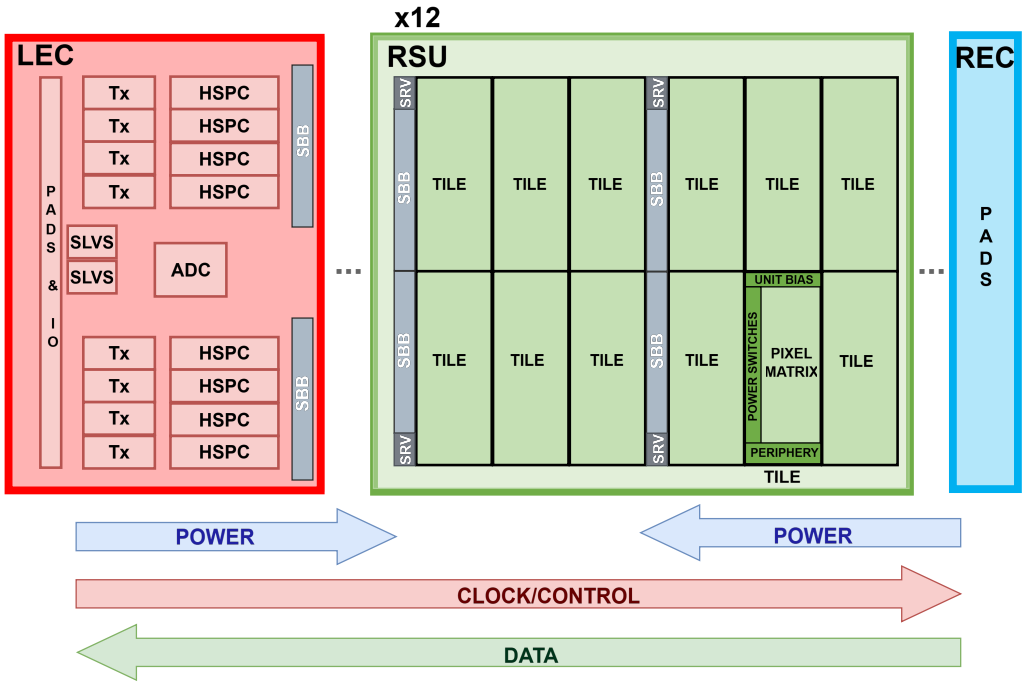

Figure 3: MOSAIX floorplan (not to scale).

The Stitched Backbone (SBB) distributes clock and performs data retiming every 10.8 mm. Each Tile has a one-to-one direct connection to the Left Endcap (LEC) via SBB, resulting in a total of 144 on-chip transmission links. Data is sent through 160 Mb/s links routed over the pixel matrices using differential transmission with a low-voltage swing. Each data link is hopped between two neighboring SBBs, as shown in Fig. 5, where the buffer $N-1$ of one SBB connects to the buffer N of the next SBB on the left. The hopping is required to allow for stitching. A 160 MHz clock is distributed from the LEC to all Tiles as a full rail-to-rail CMOS swing signal via triplicated clock buffers.

2.2 Left and Right Endcaps

The Right Endcap (REC) is a simple block that hosts the power pads and provides termination for the signals coming from the Stitched Backbone (SBB). The Left Endcap (LEC) acts as the central hub for both data aggregation and distribution of control signals. The total input bandwidth from all Tiles is 144×160 Mb/s, corresponding to 23 Gb/s. The LEC directly drives electro-optical transceivers (VTRx+) through eight high-speed serializers, interfacing with the off-detector service electronics responsible for readout, control, and power distribution [6]. The LEC supports two operating modes: a nominal data transmission of 30.72 Gb/s using three serializers at a 10.24 Gb/s line rate, or 5.12 Gb/s using six serializers. Redundant serializers are included to ensure reliability in case of both on-chip and off-chip link failures. Unused serializers are powered down. All input and output connections are placed only along the short edge of the LEC. Both LEC and REC are implemented as digital-on-top blocks.

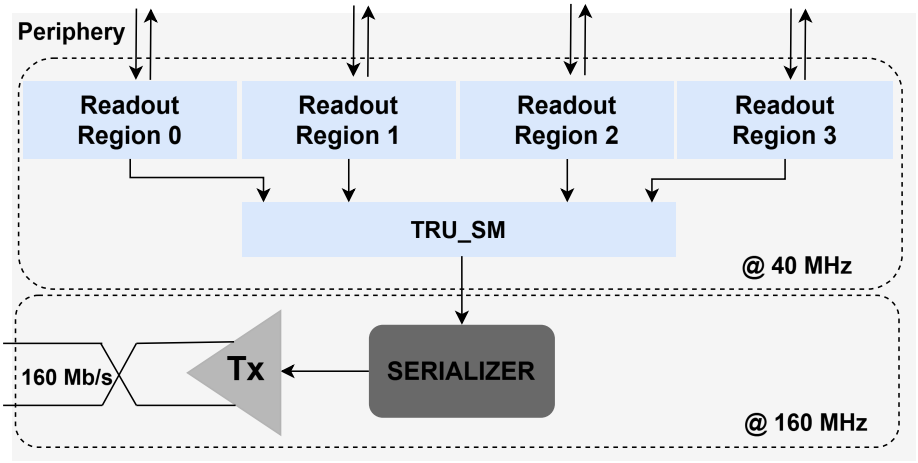

Figure 4: High-level overview of the Periphery architecture.

3. Yield and Power Distribution at Wafer Scale

To ensure high yield at the wafer scale, MOSAIX is designed to remain fully operational even in the presence of localized defects. A key feature of the architecture is its modularity, which allows faulty Tiles to be isolated from the power network without affecting global functionality. Disconnecting a defective Tile increases the dead area for 0.7% but the chip remains fully functional. This highly modular architecture minimizes the impact of single-point failures. A high priority in the MOSAIX design was to minimize the probability of shorts and to make the design as robust as possible. To achieve this, custom design rules were developed. Each building block is categorized according to its failure impact, and custom design rules are applied to each category. The higher the impact of the potential failure of the building block, the stricter the custom rules are applied. In addition, a dedicated set of custom libraries was developed for MOSAIX to improve design-for-manufacturability (DFM). These include wider metal tracks, increased metal spacing, and double contacts. An additional library flavor was created for low leakage, achieved by increasing the gate length. There is also an additional library for in-matrix cells, where the substrate is reverse-biased.

Ensuring reliable power distribution [7] across the wafer-scale sensor was one of the most critical design challenges. With all power connections confined to the short edges of a 26.6 cm-long chip, maintaining uniform supply levels across the full area required extensive analysis and optimization of the power grid. With a 1.3 V supply applied at both edges, the worst voltage drop occurs at the center of the segment, reaching 0.1 V per rail. The resulting voltage range, from 1.1 V to 1.3 V with ±0.02 V margin, is used to define the delay corners for the physical implementation, ensuring that all building blocks are simulated and verified across the expected operating conditions.

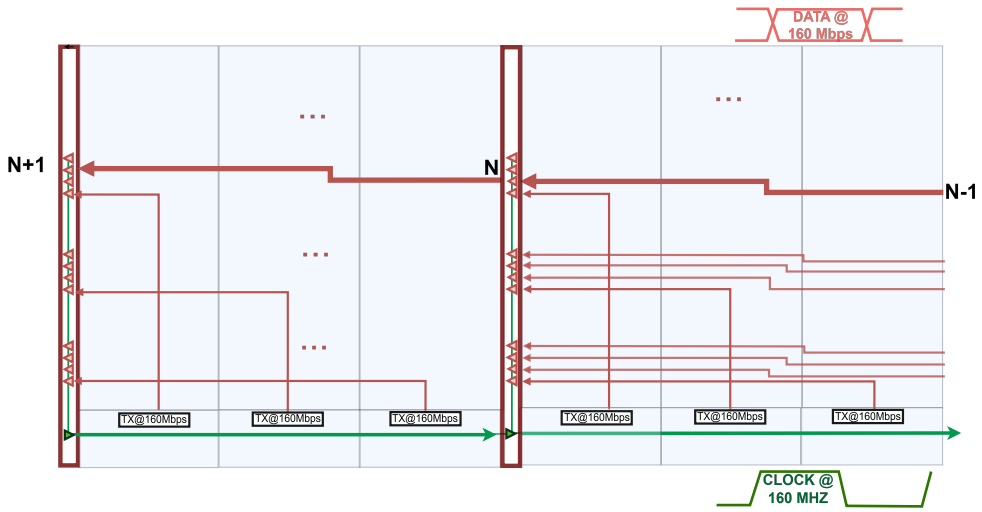

Figure 5: Connection between two Stitched Backbones illustrating data hopping.

4. MOSAIX Development and Verification

MOSAIX development builds upon the experience gained through several phases of R&D and prototyping. A series of Multi-Layer Reticle 1 (MLR1) test chips [8] were produced to validate the process technology. This was followed by the Engineering Run 1 (ER1) phase, whose goal was to evaluate stitching technology, wafer-scale yield, and overall performance [9, 10]. As the first full-scale and fully functional prototype, MOSAIX development started with an extensive R&D effort involving iterative refinements of its architecture. Several design re-spins of individual building blocks were done until all performance and integration constraints were satisfied. MOSAIX represents a major breakthrough in both scale and complexity, integrating approximately 230 million transistors per RSU and about 3 billion transistors in total.

The design and verification process presented significant challenges due to the high degree of interconnection among building blocks. Each modification in one subsystem could affect multiple dependencies, requiring careful co-design and validation. MOSAIX is implemented using a digital-on-top methodology and demonstrates the feasibility of integrating a complete detector system within a single wafer-scale sensor.

The verification of MOSAIX was performed across multiple abstraction levels, including functional, gate-level and power-aware simulations. Table 1 summarizes the scope and duration of these activities for the sign-off phase. Runtimes shown in the table are normalized to 64 cores. MOSAIX verification is run on the CERN batch computing cluster comprising 43 nodes with a total of 1528 CPU cores and 9 TiB of RAM.

5. Conclusion

MOSAIX represents a major milestone in the development of wafer-scale monolithic pixel sensors for high-energy physics. Implemented in TPSCo 65 nm CMOS technology, it demonstrates through extensive design and verification the feasibility of integrating a complete detector system within a single wafer while meeting the stringent requirements of the ALICE ITS3 upgrade. Its distributed and modular architecture enables high yield, efficient power distribution, and reliable high-speed data transmission, all within the constraints of air cooling and a minimal material budget. MOSAIX was taped out in Q3 2025. A dedicated test system [11] is being

prepared to validate functionality and performance at the wafer scale. The corresponding results will guide any necessary refinements toward the final production chip.

Category	Tests	Runtime [days]
Functional	Tile: 98k tests	78
	RSU + LEC + Segment: 10k tests	11
Gate Level	15k tests per corner	56
Power-aware	2k tests	11

Table 1: MOSAIX signoff verification runtime normalized to 64 cores.

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