PROCEEDINGS OF SCIENCE

Pixel Core Column Issue in the ATLAS Inner Tracker Modules

C. Hultquist,[a,*] L. Meng,[b] R. Bates,[c] C. Buttar,[c] G. Calderini,[d] F. Crescioli,[d] L. Cunningham,[c] Y. Dieter,[e] R. Han,[c] T. Heim,[a] S. Hirose,[f] F. Huegging,[e] D. Kim,[g] A. Korn,[i] M. Marjanovic,[j] J. Metcalfe,[g] K. Nakamura,[h] J. Pater,[k] H. Pernegger,[l] M.A.A. Samy,[c] M. Schuessler,[e] A. Sharma,[k] E. Thompson,[a] M. Backhaus,[m] J. Christiansen[l] and F. Loddo[n]

[a] *Lawrence Berkeley Laboratory, Berkeley, United States*
[b] *Lancaster University, LA1 4YW Lancaster, United Kingdom*
[c] *University of Glasgow, United Kingdom*
[d] *LPNHE, Paris, France*
[e] *University of Bonn, Germany*
[f] *University of Tsukuba, Japan*
[g] *Argonne National Laboratory, United States*
[h] *KEK, Japan*
[i] *UCL, London, United Kingdom*
[j] *University of Oklahoma, United States*
[k] *University of Manchester, United Kingdom*
[l] *CERN, Switzerland*
[m] *ETH Zurich, Switzerland*
[n] *INFN Sezione di Bari, Italy*

E-mail: charlie.hultquist@berkeley.edu

Pixel modules for the ATLAS ITk Pixel detector upgrade are currently undergoing production and quality control. During pre-production electrical testing, a recurring front-end chip communication issue was observed that could be bypassed by selectively disabling pixel core columns within the affected chips. The issue, designated as the "core column issue," has been documented across a large number of both ITkPix v1.1 and v2 modules. Since disabling a core column significantly reduces the number of operation pixels in a module, the prevalence of this failure could substantially impact ITk tracking performance.

The erratic behavior of the core column has led to difficulties in diagnosing its underlying cause. However, recent progress in visual inspection, combined with statistical analysis of production database records, points towards possible causes of the issue. This contribution highlights the discovery of, attempts to mitigate, production testing strategies, and current hypotheses of the core column issue.

VERTEX 2025 : 33rd International Workshop on Vertex Detectors 25 - 29 August 2025 Knoxville, Tennessee, USA

*Speaker

ISSN 1824-8039. Published by SISSA Medialab.

PoS(VERTEX2025)014

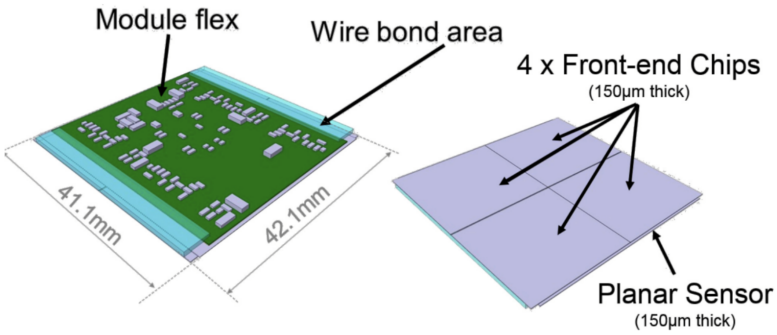

Figure 1: Model of a Quad Module during different assembly stages. Left: The fully assembled module with flex wire bonded to the sensor. Right: A bare module with four front-end chips placed onto a sensor.

1. Introduction

The High-Luminosity Large Hadron Collider (HL-LHC) upgrade to the current LHC aims to collect a total integrated luminosity of 2500 fb^{-1} over 10 years, beginning in 2030. The increased luminosity at the HL-LHC will create challenges for charged particle tracking, including a higher particle density, increased radiation damage, and increased data readout rate. To meet these challenges, the current ATLAS [1] Inner Detector will be replaced with the all-silicon Inner Tracking detector (ITk) [2], consisting of silicon pixel layers surrounded by silicon strip layers.

The ITk Pixel detector forms the 5 innermost layers of the ITk, consisting of 8,372 pixel modules. A module either comprises three (triplet) or four (quad) readout chips bump-bonded to a passive silicon sensor. This hybridization process is a particularly delicate, multi-step process where wafers are first bump-deposited, thinned and diced. The chips are then flip-chipped onto a sensor to make a bare module. The bare modules then undergo module assembly, where the readout chips are wire-bonded to a flexible PCB that is glued to the backside of the sensor. A depiction of the module at different stages in the assembly process is shown in Figure 1 High voltage is applied to create a fully depleted region inside the silicon sensor. The pixel pitch is 50×50 μm^2, except in the innermost barrel region, where pixels are 25×100 μm^2.

The front-end chip design was jointly developed by the RD53 collaboration for ATLAS and CMS [3]. The ATLAS version of the chip is referred to as "ITkPix". Each chip measures 2×2 cm^2 and consists of 400 columns and 384 rows of pixels. The basic building block of digital logic in the circuit is an 8×8 pixel region, known as a "core," and the chip is organized into 50 Core Columns (CC), as shown in Figure 2. The chip bottom controls system functionality, distributing biases, triggers, and a clock to core columns. The chip can be disabled at three different levels of granularity. An entire chip can be disabled, individual core columns can be disabled through clock gating, and the calibration injection, data readout, and HitOr trigger contribution of individual pixels can disabled.

A significant malfunction pattern, known as the "Core Column Issue," has been identified in both the pre-production (ITkPix v1.1) and production (ITkPix v2) versions of the FE chip. In some modules, when all core columns in the chip are enabled and charge is injected into the circuit, the chip will become unresponsive to triggers until the data processing chain is reset. While the issue

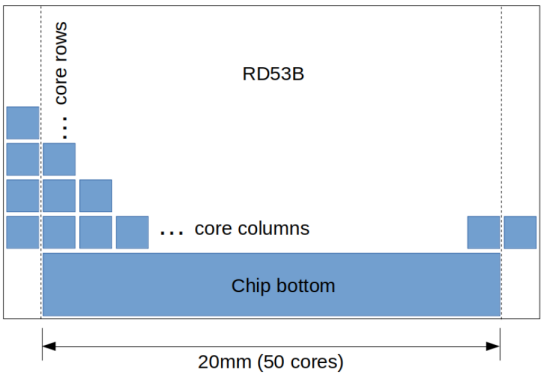

Figure 2: Conceptual depiction of RD53B framework, with a matrix composed of 50 or more columns by up to 50 rows of identical cores, and a fixed chip bottom. The same design is used in the pre-production and production version of the ITkPix chip.

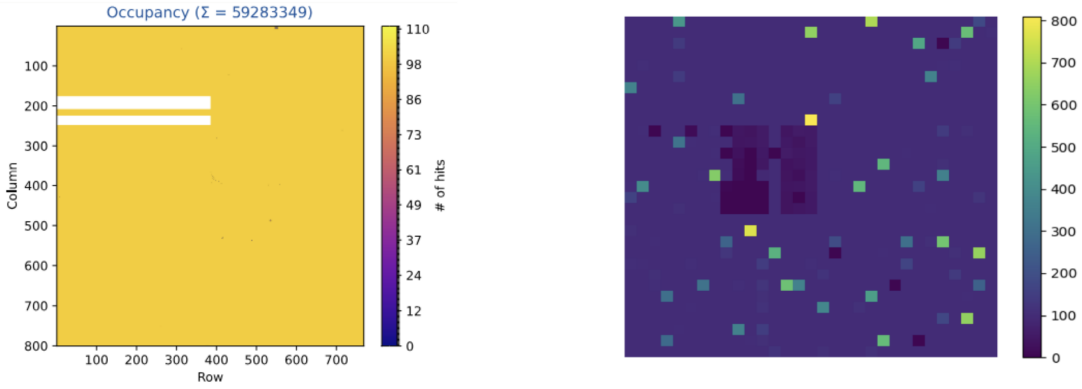

Figure 3: Left: Occupancy map of an analog scan for a quad module with core column issues in the top left chip. Entire core columns needed to be disabled for the scan to perform. Right: Analog scan for a portion of a chip with core column issues. When the dark 8×8 pixel area, a core, is disabled, the chip can function properly.

can be temporarily resolved by disabling one or more core columns, this turns off more than 2% of the active area of a chip, disqualifying a module for inclusion in the final detector. Examples of this behavior are shown in figure 3. With approximately 25% of production chips exhibiting the defect, this defect has created a significant bottleneck in production yield. Accordingly, throughout pre-production and production of the ITk pixel detector, a wide variety of studies have been done to understand and mitigate the cause of the issue.

2. Investigations

2.1 Electrical Testing

The core column issue has not been observed during front-end chip wafer probing, excluding intrinsic design flaws as the origin. The presumed cause is therefore damage to electrical circuitry

arising during hybridization or module assembly.

Initial mitigation efforts focused on identifying and disabling specific problematic pixels within affected core columns, which would deactivate less than 2% of the FE chip area and potentially qualify modules for detector inclusion. However, initial testing of the issue demonstrated cases where this was insufficient. Even when all pixels in a core column were disabled via the pixel matrix, as long as the core column remained clocked, the chip would stop communicating. In a limited number of modules, communication with the chip could resume when disabling a pixel region (4×1 pixels) or pixel core. However, these rare cases were unstable, and often different subsets of a core column needed to be disabled under different testing conditions (temperature, injected charge, threshold).

Electrical testing revealed two distinct behavioral issues associated with the core column problem. First, in a subset of cases, an FE with problematic core columns enabled will transmit corrupted data when attempting to communicate with it. This observation led to a practical diagnostic procedure in which global registers are systematically read while enabling one core column at a time. Core columns returning nonsensical values are flagged and disabled before proceeding with quality control testing. The second issue involves intermittent core column failures rather than consistent malfunctioning. This inconsistency makes these cases particularly challenging to diagnose. However, this issue occurs more frequently when chips are tuned to lower threshold values. To identify these intermittently failing core columns, after the initial global register scan, modules undergo a large number of analog injections at low thresholds, identifying core columns missed during the first scan.

The varied and erratic behavior of the core column issue during electrical testing complicates the characterization of the issue from an electrical perspective. Some affected chips still evade the current diagnostic procedure and have yet to be understood. Given these limitations, attention turned to potential physical causes.

2.2 Destructive Testing

The first confirmation of mechanical damage causing core column issues was an accidental discovery, where two previously functional quad modules developed core column issues after electrical testing on a vacuum chuck. On one module, was induced in two chips by rotating the module within the same setup. A dent was identified on the backside of one of the FE chips at the location of the disabled core columns, depicted in Figure 4. Investigations revealed a 100 μm bump from a solder splash on the vacuum chuck that caused cracking on the backside of the module when placed in the setup.

This discovery prompted a systematic inspection of the backside of modules with core column issues. Despite the promising initial evidence, many affected modules showed no large cracks or dents on the backside. Suspecting that damage between the FE chip and silicon sensor might be an additional cause, two modules with CC issues were disassembled by melting the bump bonds between the FE and sensor and using vacuum tools to separate the two pieces. Defects were found in multiple locations on both chips, but contained a 20 μm piece of material embedded between the material that coincided with the location of a dead core column. An example of this defect is shown in Figure 4. An energy-dispersive X-ray measurement revealed that the material in these

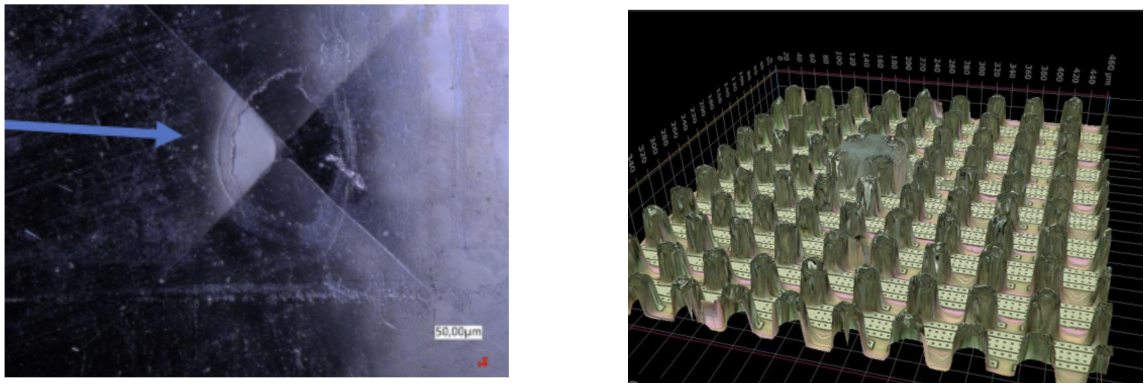

Figure 4: Left: Image of a crack and dent seen on the backside of the sensor in a module with core column issues induced by the vacuum chuck. The crack is shallow and can be seen clearly only under the correct lighting. Right: a 3D scan of the pixel matrix in a module pulled apart to study its core column issues. A 20 micron debris in the middle of the image is the piece of silicon hypothesized to cause the core column issues in this module.

defects consists mostly of silicon, suggesting debris from dicing was lodged between the FE chip and sensor during hybridization.

2.3 Hybridization Procedure Testing

The evidence from destructive testing directed investigations toward the hybridization procedure as a source of mechanical damage inducing the core column issue. The varying characteristics and frequency of core column issues across different vendors further implicated vendor-specific hybridization procedures as the cause of core column issues.

The ITk project employs three hybridization vendors, each using distinct procedures and production volumes. As seen in Figure 5, Vendor A exhibits a concentration of core column issues at edge core columns, indicating a correlation with the dicing procedure. Inspection of the pixel matrix in Vendor A chips reveals chipping in the active area from dicing blades, potentially causing the damage that triggers core column issues. To address this, Vendor A is implementing an improved dicing procedure using laser pre-grooving to create an indent before the dicing saw blade completes the cut. Early results from the two-step procedure show much cleaner dicing edges, which is a promising indicator it may reduce the prevalence of core column issues produced by this vendor.

Vendor B modules display a more uniform distribution of core column issues across the chip, suggesting contamination from dispersed debris. Notably, both modules with silicon debris trapped between the FE and sensor described in Section 2.2 came from this vendor. Multiple mitigation strategies were tested to reduce silicon debris during flip-chipping, including thinner dicing blades, enhanced visual inspection, and acetone cleaning. The most effective approach proved to be a tape-transfer cleaning procedure. In this process, after dicing (when chips remain on the original dicing tape), a fresh piece of tape is applied to the top surface of the diced chips. The contaminated bottom tape is then removed and replaced with clean tape. Finally, the top tape is peeled away, effectively removing silicon debris that adhered to the original dicing tape. Early implementation of this tape-transfer procedure shows a promising reduction in core column issue rates from this

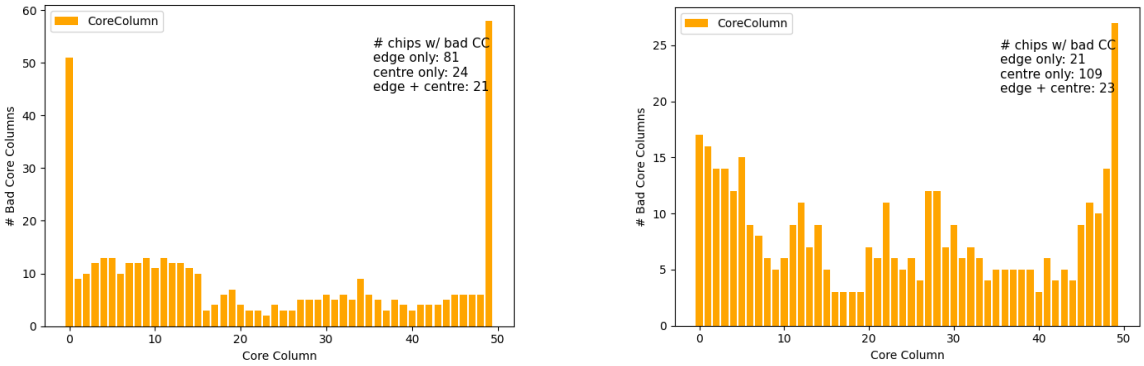

Figure 5: Left: Distribution of disabled core columns in ITkPix v2 modules produced by vendor A. Right: Distribution of disabled core columns in ITkPix v2 modules produced by vendor B.

vendor, from approximately 30% of modules containing dead core columns before the cleaning procedure was implemented, to 15% after the procedure was implemented.

Finally, Vendor C demonstrates a significantly lower prevalence of core column issues (5% of modules) compared to the other vendors (33% and 24% of modules for vendors A and B, respectively), suggesting their hybridization procedures may inherently minimize the mechanical damage causing this problem. With the implementation of laser pre-grooving at Vendor A and the tape-transfer cleaning procedure at Vendor B, the overall incidence of core column issues is expected to decrease substantially as production continues. These targeted improvements across vendors should significantly enhance module yield for the remainder of the ITk production phase.

3. Core Column Issues in the ITk

Although the mitigation strategies developed with hybridization vendors are promising, the improvements were implemented after production began, resulting in many modules already manufactured with core column issues. Additionally, some core column issues manifest only after extensive testing, suggesting that latent problems may appear after ITk installation. It is therefore crucial to understand the long-term behavior of these issues and their effect on detector performance.

Comprehensive studies are underway to evaluate the progression of core column issues under operational conditions. Pre-production quality control was conducted across multiple sites under varying conditions. It is difficult to conclude the long-term behavior of the core column issue due to this variability. To address this, the ITk project will perform systematic stability testing on a sample of production modules with core column issues. Tests include thermal cycling, long-term operation, and radiation exposure. The issue is also being monitored as modules are integrated onto local support structures.

Initial simulations assessing the impact on tracking performance are ongoing, but early results indicate that track resolution remains relatively unaffected unless more than 15% of core columns are disabled across the ITk. The detector's robust design provides substantial tolerance for active area loss. Additional studies are ongoing to fully characterize the physics impacts of core column failures.

4. Conclusions

The core column issue represents a critical malfunction during the operation of the ITkPix FE chip, where the chip becomes unresponsive to triggers after charge injection unless affected core columns are disabled. This issue impacts approximately 25% of production modules. Electrical testing revealed potential dependency with the chips analog settings and allowed for the development of diagnostic procedures to identify core column issues. Visual Inspection and destructive testing confirmed mechanical damage as the root cause, with hybridization procedures identified as the primary source. Discussions with vendors have yielded procedural improvements that partially mitigate the issue, though the long-term effects under thermal stress and radiation exposure remain under investigation.

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, Journal of Instrumentation **3** (2008) S08003. doi:10.1088/1748-0221/3/08/S08003.

[2] C. Buttar for the ATLAS ITk Collaboration, *ATLAS ITk pixel detector overview*, Nuclear Instruments and Methods in Physics Research Section A (2024). doi:10.1016/j.nima.2024.169978.

[3] RD53 Collaboration, *RD53 pixel readout integrated circuits for ATLAS and CMS HL-LHC upgrades*, Journal of Instrumentation **20** (2025) P03024. doi:10.1088/1748-0221/20/03/P03024.

PoS(VERTEX2025)014