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^{60}Co γ Irradiation of the CMS CROC v2 to 1.6 Grad

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This paper reports the irradiation of the production version of the readout chip for the CMS HL-LHC pixel detector, CROC v2, to 1.6 Grad using γs from a ^{60}Co source at Sandia National Laboratory. The CROC v2 was kept powered, configured, and maintained as close as possible to its nominal operating temperature of -20 ^{o}C during irradiation. Internal chip voltages, pixel response, and diagnostic ring oscillators were continuously monitored, and thresholds were optimized frequently. The CROC v2 performed according to specifications at 1.6 Grad. Where available, these results will be compared with those for this and earlier iterations of the RD53 readout chip irradiated to a few Grad with lower-energy X-ray sources.

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1. Introduction

Silicon pixel detectors are essential components of particle-tracking systems in the Large Hadron Collider (LHC) experiments. They provide high-precision, three-dimensional hit information in high-radiation regions closest to the proton-proton collision points. For the High-Luminosity LHC (HL-LHC) upgrade of the Compact Muon Solenoid (CMS) detector [1, 2], the innermost tracking layers must withstand an unprecedented total ionizing radiation dose (TID) of up to 1 Grad over 10 years [3]. The hybrid pixel detectors are made of two separately produced components: a silicon sensor layer and a readout chip (ROC), connected via bump-bonding. Testing sensors and ROCs with radiation doses up to and beyond 1 Grad is crucial to assess the detectors' viability. A radiation-tolerant pixel ROC for ATLAS and CMS was designed within the RD53 collaboration at CERN [4]. The team selected commercial 65 nm CMOS technology and first developed a half-sized demonstrator chip, the RD53A, to evaluate different front-end architectures. Several x-ray irradiations and one ^{60}Co γ irradiation campaign established that it can tolerate radiation doses up to 1 Grad. RD53 then designed full-scale production versions for each experiment: the ITkPix for ATLAS and the CROC for CMS [5]. Although optimized for their respective detectors with minor differences in size and analog front-end, the chips share a common architecture.

Gamma rays simulate high-penetration radiation effectively. They cause ionization, leading to the creation of electron-hole pairs in the silicon dioxide layers (gate oxides, shallow trench isolation (STI) oxides, and spacers) of transistors. Trapped positive charges build up in these oxides, resulting in performance issues such as threshold voltage shifts and drain current [6, 7]. Gamma irradiation ensures the entire device, including the bulk silicon, STI regions beneath the active layers, and the packaging, receives a uniform TID. The first irradiation of the production version of the CMS readout chip (CROC v2), with 1.17 and 1.33 MeV photons from a ^{60}Co source, was conducted at the Gamma Irradiation Facility (GIF) of Sandia National Laboratory. This paper describes the experimental setup and electronic tests conducted during continuous exposure of the readout chip. We discuss the results and failure modes observed during scans. We conclude with an assessment of the electronics' viability after irradiation to a total dose of 1.6 Grads.

2. The CROC v2 Readout Chip

The CROC v2 [5] has 145,152 readout channels with a 50 μm by 50 μm pitch over an area of about 4 cm^2. The pixel front-end includes a charge-sensing amplifier with Krummenacher feedback in the analog front-end, 4-bit charge information with a 40 MHz time-over-threshold (ToT) measurement in the digital front-end, and 5 bits of in-pixel configuration for threshold equalization. Data is transmitted from the chip via up to four high-speed serial links (1.28 Gb/s).

The CROC v2 features two on-chip banks of ring oscillators built with different standard cells and drive strengths. The transistor drive strength is related to the size of some transistors in the circuit, where strength-zero gates utilize minimum-size transistors, while other strength gates do not. In ring oscillators, an odd number of logic inverters are connected in a loop, generating continuous oscillations whose frequency depends on the properties of the transistors and interconnects on the chip. The gate delays of the ring oscillator are affected by the TID.

The CROC v2 for this study was produced by Taiwan Semiconductor Manufacturing Company (TSMC) in late 2023 for an engineering run and delivered in January 2024. It is labeled number 66 on wafer 16E6, which is one of 20 wafers produced. The wafer-level testing was performed at the INFN/University of Torino, Italy [8]. This included testing the functionality of the chip's power-consuming components. The chip's main voltages were set to the nominal 1.2 V, and the reference current was adjusted to approximately 4 μA, used for several analog components. During the wafer-level probing, each CROC was subjected to many of the same function tests and calibrations that it will undergo during operation. The CROC v2 under study passed all tests. The average yield for CROC v2 chips in the engineering run was reported at about 80 % [8].

There are 136 CROC v2s on a 12-inch wafer, and after dicing, a small portion was sent to Purdue University for attachment to Single Chip Cards (SCCs) shown in Fig. 1. The card measures 10 cm on each side, and the CROC is glued onto an aluminum plate, which is then attached to the card. The CROC is positioned on the vertical centerline of the card, above the horizontal centerline. At the bottom of the CROC, 194 wire bonds connect pads on the CROC to corresponding pads on the irradiation card, providing voltages, grounds, command lines to the chip, and digital signals from the chip. The SCC was coated with a 14 μm thick parylene-N layer with all connectors masked.

The SCC is connected to the CMS FC7 data acquisition (DAQ) and control application [9], built around a Xilinx Kintex-7 FPGA, via a 7 m Display Port cable. Power for the analog and digital components of the CROC v2 is supplied via a Molex connector with two low-voltage and two ground pins, located at the bottom-left side of the SCC. The CROC's voltages, currents,

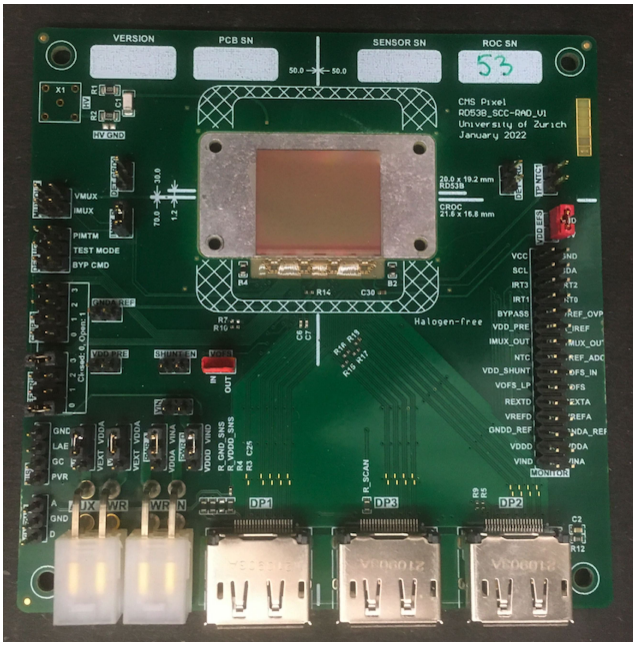

Figure 1: A CROC v2 mounted on a Single Chip Card designed by the University of Zurich and wire-bonded to pads on the irradiation card.

and temperatures can be monitored through pin connectors. The availability of these multiplexed

(MUX) data depends on the CROC being adequately powered and operational. A Keithley 2400 SourceMeter connected to dedicated pins on the SCC digitizes and transmits the information to the DAQ computer. A portion of the chip's internal voltages can also be measured from the large pin block on the right side of the SCC, even if the CROC isn't adequately powered or fully configured. Only the MUX data was monitored during the irradiation.

3. Cooling System

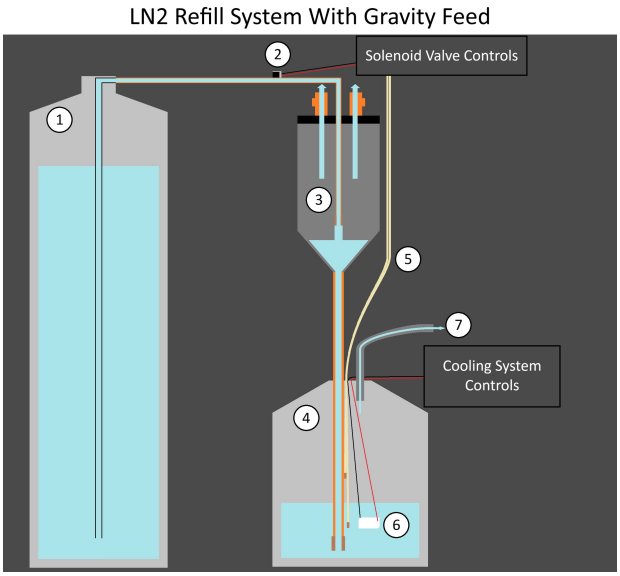

Figure 2: Schematics of the cooling and refill system. A small Dewar is periodically filled with liquid nitrogen, from which cold nitrogen gas is produced and flows into the thermos containing the SCC. (1) The large liquid nitrogen reservoir Dewar. (2) The solenoid-controlled valve maintains levels of liquid nitrogen in the small Dewar. (3) Gravity feed with check valves to ensure the flow rate into the small Dewar does not cause overcooling of the electronics. (4) The small Dewar where the liquid nitrogen is boiled off to cool the electronics. (5) The liquid nitrogen sensors used by the solenoid valve controls measure the nitrogen level in the small Dewar. (6) The resistor used by the cooling system controls to boil off cold nitrogen. (7) The transfer line to transport cold nitrogen gas to the thermos holding the electronics in the irradiation cell.

The SCC is placed inside a cylindrical thermos made of double-wall-vacuum stainless steel. During irradiation, the thermos is surrounded by ^{60}Co rods. An ion chamber is temporarily placed inside the thermos to measure the dose. The cooling system for the irradiation was a nitrogen boil-off system that kept the electronics cold and dry for over three weeks without interruption, meeting the strict requirements of the Sandia GIF. Evaporated nitrogen flows from a small Dewar through a transfer line to the CROC v2 thermos, cooling the electronics, then exits the system into the irradiation cell. Dryness was particularly challenging because the electronics were placed above a water pool used for storage of the ^{60} Co rods when not in use. The system blows dry, cold nitrogen over the electronics. The controls are programmed in LabVIEW. The liquid nitrogen boil-off system is shown in Fig. 2. The large Dewar was refilled about every 2.5 days. This ensured

an uninterrupted operation over weekends without the need for access. The temperature of the readout chip was measured using a K-type thermocouple placed between the aluminum plate to which the CROC v2 is glued and the thermal putty, which conducts heat to a copper plate serving as a heat sink. The card's temperature was maintained within .03 °C at -20 °C 95 % of the time.

4. Chip Performance Measurements

Front-end scans were performed regularly to detect anomalies in the chip's front-end circuitry, including those carried out during wafer probing. Scans are implemented in the Ph2_ACF software framework [10]. To determine the oscillation frequency in the ring-oscillator circuit, the output is connected to a counter. The *ring-oscillator scan*, after a period equivalent to 50 bunch crossings (1.25 μs), stops the oscillators, and records the counts.

The CROC v2 can inject a programmable amount of charge into each pixel's front-end electronics. This simulates the signal from a particle hit without requiring an external radiation source. A *pixel-alive scan* checks whether each pixel responds. The CROC v2's analog front-end consists of a charge-sensitive amplifier and a comparator in each pixel. Analog scans test and calibrate these circuits. The pixel's efficiency is measured as a function of the injected charge, following a sigmoid function (S-curve). The point at which a pixel reaches 50% efficiency defines its threshold—the minimum charge required to trigger a response—and the width of the S-curve measures the pixel's noise level. The *threshold-tuning scan* adjusts the overall chip threshold to achieve approximately 1,000 electrons per pixel. A separate scan is used to equalize the threshold and response across the entire pixel matrix, ensuring uniform performance. The process involves setting a global threshold for all pixels on a readout chip, and then fine-tuning individual pixels [5].

The CROC v2 measures the input charge using a 4-bit Time-over-Threshold (ToT) counter. A *ToT scan* characterizes the linear relationship between the injected charge and the measured ToT value. A register allows adjustment of the ToT interval length.

A *MuxScan* transmits on-chip voltages to the Keithley voltmeter, where they are recorded. Various internal voltages and the supplied current were scanned before and during irradiation.

5. Irradiation Results

The irradiation lasted 25 days, beginning on July 9th, 2024, at 13:15 and finishing on August 2nd. The dose rate as measured by a well-calibrated ion chamber at the start of the irradiation was constant 775 Rads/second with a dose rate difference between the top and bottom of the chip of about 11 Rads/second. Fairly consistent communication with the chip continued through August 2nd at 16:10 until a failure of the cooling system ended the irradiation.

The ring-oscillator, MUX, and charge-injection scans described in Sec. 4 were conducted every 15 minutes. Additionally, the time over threshold was frequently monitored and adjusted. This was followed by Analog and S-curve scans while being tuned to a threshold of 1000 electrons, which corresponds to a calibrated value (Delta VCAL) of about 182. Fig. 3 shows the mean and standard deviation of the threshold distribution for several scans versus TID.

The ToT, measured in cycles of a 40 MHz clock, is optimized by frequently adjusting an internal register (DAC_KRUM_CURR_LIN) to reach a ToT of 5.7 for 6000 injected e^-, as shown

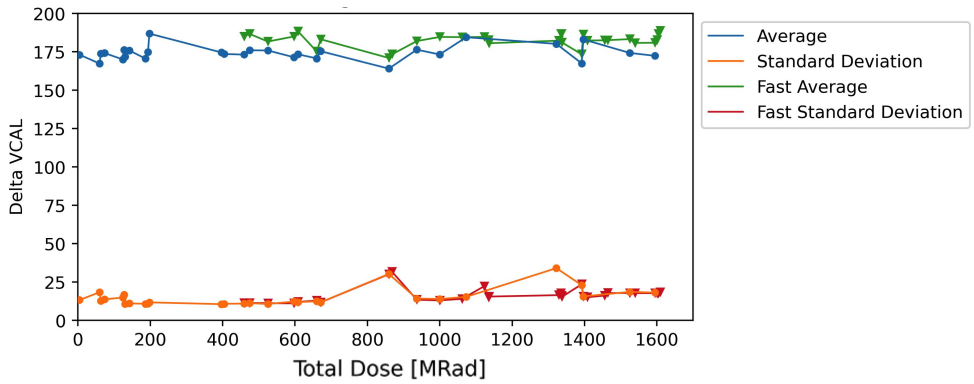

Figure 3: The average and standard deviation of all pixel thresholds after tuning to 1000 electrons, versus TID. Fast tuning scans use fewer charge injections per pixel, reducing execution time.

in Fig. 4. The relative (percentage) change of the gate delay in the ring oscillators with respect to

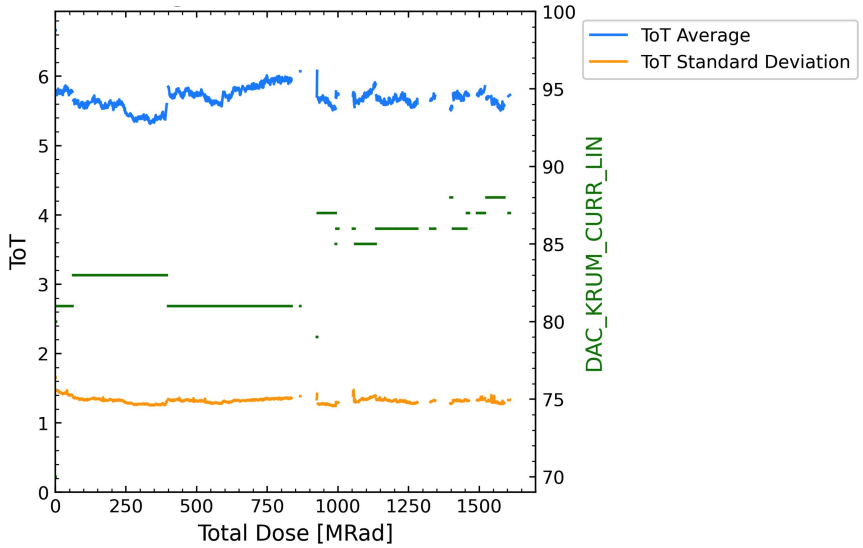

Figure 4: The average and standard deviation of all pixel ToT 25 nS cycles. The Krummenaker feedback current register (DAC_KRUM_CURR_LIN) was frequently adjusted to maintain a average ToT of about 5.7 cycles. The green points are the Krummenacher register values.

the pre-irradiation ring oscillator counts is shown in Fig. 5. The subset of bank A ring oscillators with drive strengths of zero is shown, which features the smallest size transistors.

MuxScans were performed up to a TID of 730 MRad. Afterward, the MUX wire connection to the SCC shorted out due to condensation outside the thermos, which corrupted the multiplexer readout. The internal voltages of the CROC v2 stayed within 2% of their pre-irradiation values before the read-out failed. This contrasts with other recent X-ray irradiations[11], which show larger relative percent changes at this stage of their irradiations. However, this difference between X-ray and gamma irradiations has been observed previously [12]. The multiplexer readout was

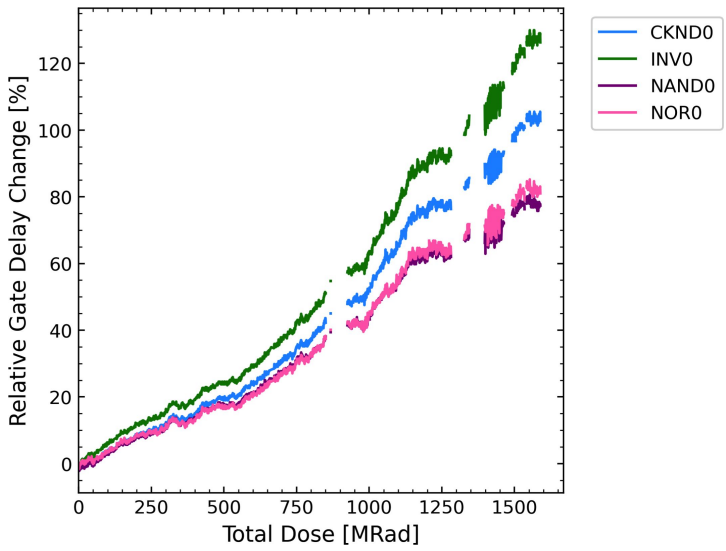

Figure 5: The relative gate delay for four ring-oscillators of strength zero, throughout the irradiation. The relative gate delay percentage is calculated with respect to pre-irradiation ring oscillator counts.

later restored in the laboratory with dry wires and a new SSC, and the observed failure, attributed to water penetrating a cable, was confirmed by dampening the cable. This test also confirmed that there is no link between the failed multiplexer readout and the actual voltages on the chip.

6. Discussion

The CROC v2's thresholds and ToT were adjustable up to the final TID of 1.6 Grad. Simulations of the chip showed that the gate delay increase must stay below 200 % to maintain good timing in the digital logic. After irradiation to 1.6 Grad, the subset of bank A ring oscillators with zero drive strength displays a wide range of relative gate delays between 80 and 130 % (see Fig. 5). For Bank A with drive strength four, the change is between 40 and 55 %. Similar irradiation effects on ring oscillators have been observed with X-rays at TID levels up to 2.3 Grad [11]. Over the detector's lifespan, which corresponds to a TID of 1 Grad, the lowest strength electronics will experience a maximum relative gate delay increase of 64 %. An increase of over 200 % in relative gate delay is not expected, even if possible rate-dependent effects with factors of 2.3-3 are included [12].

7. Conclusions

A CROC v2 readout chip, mounted on a single-chip card, was irradiated with gamma rays from ^{60}Co at Sandia National Laboratory up to a TID of 1.6 Grad while kept at -20 °C. Despite a significant increase in gate delays in built-in ring oscillators, the chip remained operational and met overall system requirements. Similar relative changes in gate delays of ring oscillators have been observed with X-rays at these TID levels. These results indicate that the CROC v2's logic gates will function in the detector throughout their expected lifespan. Furthermore, due to the parylene coating, no damage to wire bonds was observed after exposure to radiation and humidity.

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