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Sensor and Module Development for the CMS Phase-2 Tracker Upgrade

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The CMS Phase-2 tracker upgrade relies on a new generation of silicon sensors and modules designed to perform reliably under the extreme conditions at the HL-LHC. This contribution provides an overview of the R&D, prototyping, and pre-production phases for both pixel and strip detector modules. We discuss sensor technology choices, front-end hybrid development, and innovations in powering and readout architectures. Emphasis is placed on performance validation through laboratory testing and beam campaigns, as well as the scaling up to industrialized production and the strategies adopted for quality assurance and integration into larger structures. The progress and lessons learned during module construction and early integration are presented, with a focus on meeting the demanding requirements for data rates, radiation hardness, material budget, and long-term reliability.

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1. Introduction

The LHC at CERN will enter into the high-luminosity era in 2030 targeting peak luminosities of $5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1} and integrated luminosities of $3000 - 4000$ fb^{-1}. To cope with the challenging environment characterized by high pile-up conditions, approximately 200 events per bunch crossing, and intense radiation levels, the CMS [1] tracker is undergoing a major Phase-2 upgrade [2] [3]. The Inner Tracker (IT) will cover an area of 4.9 m^2 containing 2×10^9 pixels in the innermost part of the tracking volume. Further out, the Outer Tracker (OT) will have an active area of 192 m^2, comprising 1.7×10^8 macro-pixels and 42×10^6 strips. The upgraded detector will feature enhanced granularity and extended acceptance, increasing the pseudorapidity coverage from $|\eta| \approx 2.5$ to $|\eta| \approx 4$. An overview of the detector layout is presented in Fig. 1. Furthermore the material budget will be reduced and tracking information will be propagated to the Level-1 (L1) trigger.

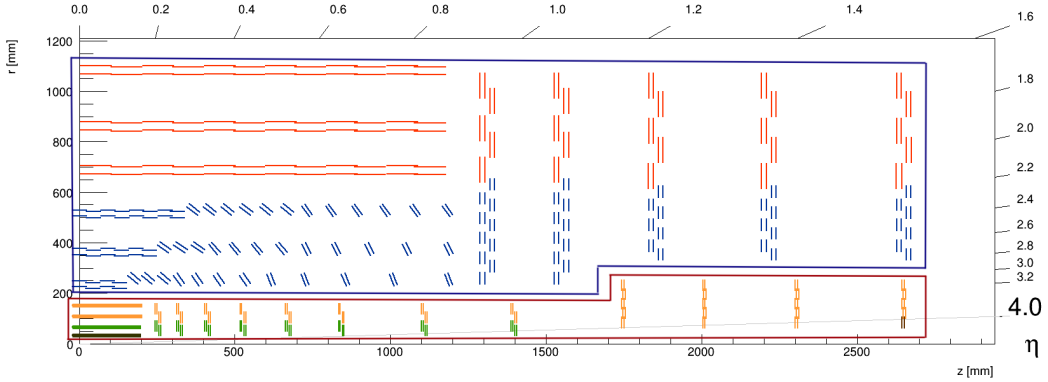

Figure 1: Layout of the CMS Phase-2 Tracker. The IT corresponds to the area outlined in red and the OT corresponds to the area outlined in blue.

2. Inner Tracker upgrade

The IT is composed of three regions: the Tracker Barrel PiXel (TBPX), the Tracker Forward PiXel (TFPX) and the Tracker Endcap PiXel (TEPX). The TBPX consists of four layers with the innermost being replaceable. The TFPX will be equipped with eight small double-disks on each end, while the TEPX features four large double-disks on each end. The innermost ring of disk four in the TEPX is dedicated to luminosity measurements.

The upgraded IT will employ two different silicon sensor technologies: 3D silicon sensors produced by Fondazione Bruno Kessler (FBK) and planar sensors manufactured by Hamamatsu Photonics K.K. (HPK). The 3D sensors will be installed only in the innermost layer of the TBPX to benefit from their lower power consumption which in turn reduces the risk of thermal runaway. The hit efficiency of the 3D sensors is required to exceed 96 % at normal incidence after irradiation and this has been successfully demonstrated up to a fluence of $\Phi_{eq} = 1.6 \times 10^{16}$ cm^{-2} [4]. The planar sensors, which are of n-in-p type, have demonstrated a hit efficiency greater than 99 % at a fluence of $\Phi_{eq} = 1 \times 10^{16}$ cm^{-2} [5]. Both planar and the 3D sensors have an active thickness of 150 µm and a pixel size of 25×100 µm^2.

The silicon sensors will be read out by the CMS Readout Chip (CROC), a 65nm CMOS ASIC developed within the RD53 collaboration. The first version, RD53A, was a half-size demonstrator that integrated three different Analogue Front Ends (AFEs) for evaluation (synchronous, linear, and differential). The subsequent full-sized version, RD53B (CROCv1) incorporated the linear AFE which was selected as the optimal design for the CMS IT. The final version, RD53C (CROCv2), features a matrix of 432×336 pixels with a cell size of 50×50 µm^2. It includes a linear AFE with an adjustable threshold to values below 1000 e$^-$ and supports time-over-threshold measurements at 40 MHz. It is equipped with on-chip Shunt-LDO regulators to enable serial powering and it is designed to be radiation tolerant up to 1Grad [6].

Different combinations for the number of CROCs per sensor are used in the IT subsystems. In the TBPX, three module types are used, planar double modules consisting of one sensor and two CROCs, planar quad modules with one sensor and four CROCs and 3D double modules containing two sensors and two CROCs. The TFPX is equipped with planar quad and double modules, whereas the TEPX hosts only planar quad modules.

The choice of serial powering allows to minimize the material budget while allowing to provide 50 kW of power to the modules. The IT will include more than 500 power chains, each capable of powering up to 12 modules in series. Data from the modules will be transferred to the low-power GigaBit Transceiver (lpGBT) [7] via e-links operating at 1.28 Gbps, while command signals will be sent from the lpGBT to the modules at 160 Mbps. The lpGBTs are integrated into dedicated portcards alongside the Versatile Transceiver plus (VTRx+) [8] which performs electrical to optical conversion of the data. The optical data is then transmitted via fibres to the Data, Trigger and Control boards (DTC) [9]. A schematic overview of the IT electronics system is presented in Fig. 2.

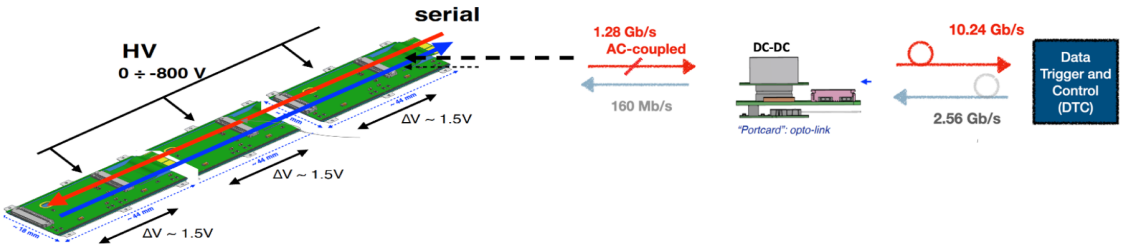

Figure 2: IT power distribution and data transmission architecture.

The module assembly process begins with bump-bonding the sensor to the CROC to form a bare module. For the TBPX modules, a cooling plate is then attached to the bare module. Next, a High-Density Interconnect (HDI) printed circuit board, is glued to the bare module providing power as well as data transfer from and command distribution to the module. In some assembly centers, this gluing step is performed using robotic arms to ensure higher precision. For the TEPX modules, the HDI gluing is taking place after an airex frame is attached to the HDI which acts as support structure. Electrical connections are then established via wire bonding. The final step involves applying parylene coating for spark protection. A simplified IT module design is presented in Fig. 3.

Throughout the assembly process, visual inspections and electrical tests are conducted to assess the module quality. The modules also undergo a burn-in test, which includes 10 thermal cycles

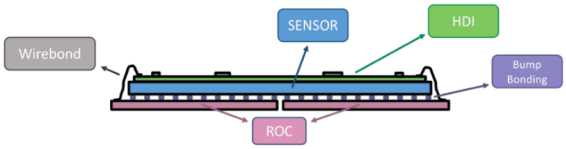

Figure 3: Structural layout of a typical IT module

from 40 °C to –35 °C. The electrical qualification involves various scans. Power tests are performed to verify the input, analogue and digital voltages of the CROC, while an I-V characteristic curve is obtained to assess the sensor quality. The testing routine includes threshold tuning scans to achieve a uniform pixel response as well as pixel-alive scans conducted before and after tuning to identify and mask problematic pixels. Additionally, bump connectivity is tested through a crosstalk-based method to detect disconnected bump bonds [10].

During module production, several types of defects were identified in the IT modules. Broken bump bonds were detected in some modules, and investigations revealed that one of the primary causes was the use of suboptimal bonding jigs during hybridisation. Other issues included damaged wirebonds and contamination on top of the connectors. These problems were traced back to the coating process and were subsequently mitigated by optimizing the coating procedures and applying masking to the critical areas.

The module assembly and testing processes are distributed across more than ten institutes within the CMS collaboration to produce the almost 4000 modules needed for the construction of the CMS IT.

3. Outer Tracker upgrade

One of the primary design drivers of the OT was the requirement for the detector to provide tracking information to the CMS L1 trigger. In order to limit the data volume transmitted at 40 MHz, a local data reduction is performed at the module level, through the p_T-module concept. Each OT module consists of two closely-spaced sensors, whose hits are correlated to form "stubs", track segments with p_T exceeding a predefined threshold. Selecting stubs with $p_T > 2$ GeV achieves a data volume reduction of around one order of magnitude, enabling stub transmission at 40 MHz.

The OT consists of three subsystems: the Tracker Barrel with Strip-Strip (2S) modules (TB2S) assembled in ladders, the Tracker Barrel with Pixel-Strip (PS) modules (TBPS) organised in planks and rings and the Tracker Endcap with Double - Disks (TEDD) which are composed by D-shaped parts, called dees which contain both 2S and PS modules. The 2S modules are available with two different sensor spacing of 1.8 and 4 mm, whereas the PS modules are available in three spacing variants of 1.6 mm, 2.6 mm, and 4.0 mm, as illustrated in Fig. 4. The variation in sensor spacing, along with the adjustable acceptance window for stubs implemented in the ASICs, ensures coherent p_T filtering across the entire OT volume. The sensors used in the OT modules are float zone n-in-p type with an active thickness of 290 µm produced by HPK.

Each 2S module consists of two micro-strip sensors, each measuring 10×10 cm^2 and containing two matrices of 1016 strips with a strip size of 5 cm $\times$ 90 µm [11]. The sensors are read out

via two 2S Front-End Hybrids (2SFEH), a left and a right variant, which are also available in two spacings. Each 2SFEH hosts eight CMS Binary Chips (CBC) produced in a 130 nm process with 254 channels per chip [12]. The CBCs are responsible for the readout of both sensors and for stub finding. Additionally, each 2SFEH includes a Concentrator Integrated Circuit (CIC), fabricated in a 65 nm CMOS process, to aggregate the data from all CBCs and perform clustering and zero suppression of the triggered data [13]. Data from the CIC are transmitted to the lpGBT which in turn forwards the data to the VTRx+ at 5.12 Gb/s. The VTRx+ performs electrical-to-optical data conversion and transmits the optical signals to the back-end electronics. Both VTRx+ and lpGBT are mounted on the 2S Service Hybrid (2SSEH), which also hosts two DC-DC converters that reduce the input voltage to the one required for the ASICs, the VTRx+, and the lpGBT. This approach reduces the current and helps maintain the material budget of the services at acceptable levels. Finally, a ground balancer circuit connects the two 2SFEHs to ensure ground equalization. The 2S modules will be exposed to radiation levels up to 4.9×10^{14} n_{eq}/cm^2 [14].

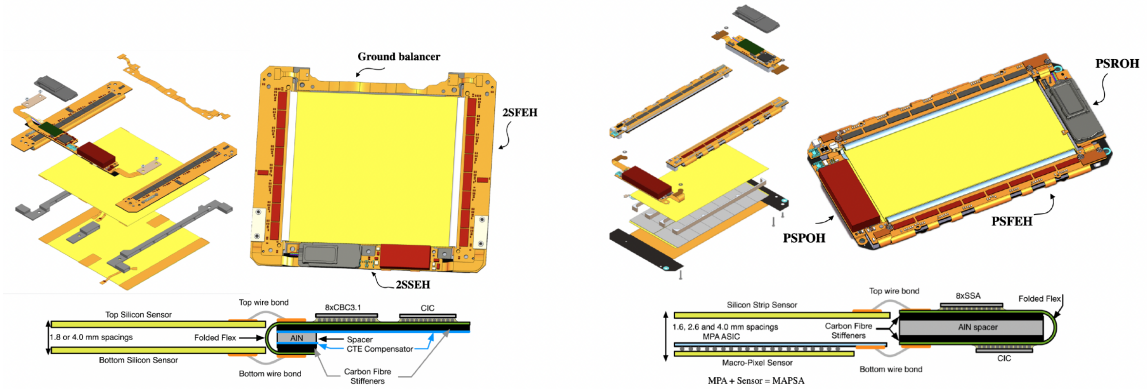

Figure 4: 2S (left) and PS (right) module designs, highlighting key components and assembly details.

Each PS module comprises one micro-strip sensor and one macro-pixel sensor, each measuring 5×10 cm^2. The strip sensor contains 2×960 strips with a strip size of 2.5 cm $\times$ 100 µm while the pixel sensor has 32×960 pixels, each sized 1.5 mm $\times$ 100 µm. The strip sensor is read out via two PS Front End Hybrids (PSFEH), a left and a right variant, each hosting eight Short-Strip ASICs (SSAs) developed in a 65 nm process [15]. The pixel sensor is bump bonded to 16 Macro-Pixel ASICs (MPAs) [16], collectively forming a Macro-Pixel Sub-assembly (MaPSA), which interfaces with the PSFEHs. The MPAs manage the pixel sensor readout and, by combining the strip data provided by the SSAs, perform the stub finding logic. The MPAs also send data to the CIC. The stub data, aggregated over two consecutive bunch crossings, are transmitted at 1.6 Gb/s, while the raw strip and pixel data are sent at 320 Mb/s upon reception of a L1 trigger. In the PS modules, clustering and the zero suppression are performed by the MPAs [17]. The CIC transmits the data to the lpGBT which forwards it to the VTRx+ at rates of either 5.12 Gb/s or 10.24 Gb/s. The lpGBT and the VTRx+ are mounted on the PS Readout Hybrid (PSROH). Due to the smaller size of the PS module the powering is provided by a separate hybrid the PS Power Hybrid (PSPOH) which hosts the DC-DC converters. The PS modules will be exposed to radiation levels up to 1.4×10^{15} n_{eq}/cm^2.

During the prototyping phase, the designs of several hybrids were evaluated to select the optimal configuration for best module performance. For the 2S modules two different 2SSEH designs were

produced, the common plane design featuring a single ground layer for DC outputs and switching power currents, and the split plane design with a separate ground for DC and switching currents, connected to a common point. The effect of the ground balancer was also assessed for both 2SSEH designs. Noise measurements on the modules indicated that the optimal configuration was the common plane 2SSEH design combined with the presence of the grounding balancer. A similar study was conducted on the grounding scheme of the PSPOH modules where one variant included the use of a zig-zag powering tail connecting the PSPOH and the PSROH. No significant difference in noise levels was observed between the two grounding schemes. Therefore, for consistency, the common plane design was adopted and the zig-zag tail was not considered necessary. Additionally, a design modification was implemented for the PSPOH hybrids after oscillations were detected in the output of one of the DC-DC converters during operation at cold. The PSPOH remote sensing scheme was optimized to eliminate these oscillations [18].

The assembly process of the 2S modules begins with the metrology of the sensors, which are subsequently insulated with kapton strips in the contact regions with the Al-CF bridges. These bridges serve as the separation material between the two sensors. The next step involves gluing and wirebonding the high voltage tails to the back side of the sensors. The two-sensor assembly is then prepared by gluing the bridges while ensuring precise sensor alignment. The hybrids are glued to the side bridges, followed by wirebonding of the 2SFEH to the sensors, along with encapsulation. For the PS modules, the assembly process is similar with the difference that they are built on a CF baseplate. A high voltage tail is attached to the strip sensor, which is layered with the MAPSA via AlN spacers. The sensor assembly is glued onto the baseplate together with the hybrids, followed by wirebonding and encapsulation. Throughout module assembly, visual inspection, metrology and electrical tests (I-V curves, noise measurements) are performed to evaluate the module quality. Additionally, a module burn-in procedure is conducted, which includes thermal cycling for 48 hours from 20 °C to -35 °C, alongside electrical testing.

During hybrid production, several types of defects were identified, Fig. 5. In the PS hybrid variants, flex delamination manifested as bulges on the flex surface. Cross-sectional analysis confirmed internal layer separation, and lead to improvements in the drying process of bare flex circuits to minimize the humidity contribution to this effect. Another issue on the PSFEH was

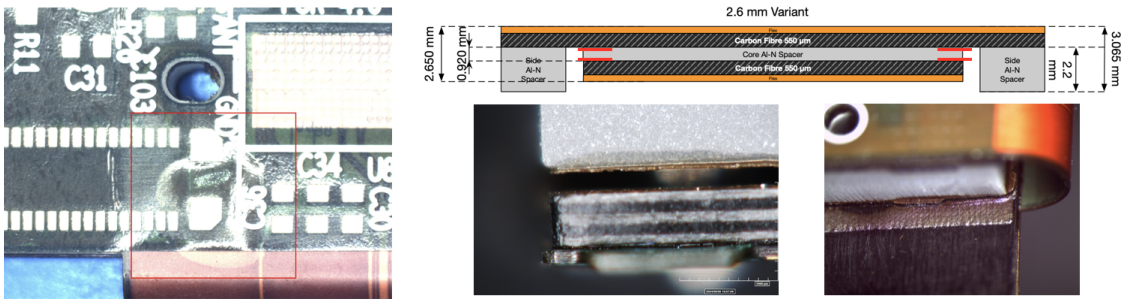

Figure 5: Delamination-induced bulges on the flex surface (left) and failures between the spacer and stiffener assembly of a PSFEH (right).

the development of cracks at the interface between the stiffener and spacer in the hybrid assembly. This damage occurred after the hybrids were subjected to elevated temperatures during the reflow

soldering process. Alternative adhesive methods are currently being investigated to resolve this problem. Additionally, contamination was detected on the wirebonding pads of the FEHs, which affects wirebonding quality. The primary source of contamination was traced to the ultrasonic cleaning bath used during hybrid production; cleaning agents became trapped in cavities within the hybrid spacer and subsequently escaped through vent holes, contaminating the pads. Design modifications to the spacers are under consideration to mitigate this issue.

The OT module production is distributed among 12 different institutes with the production rates for the 2S modules increasing, while issues related to the PS hybrids are being addressed. In parallel, the construction of larger-scale components has commenced with initial units illustrated in Fig. 6. The first fully integrated TB2S ladders have undergone successful mechanical and thermal validation. For the TBPS rings and planks, the grounding scheme is currently under evaluation, while for the TEDD dees, the module integration process has been successfully validated.

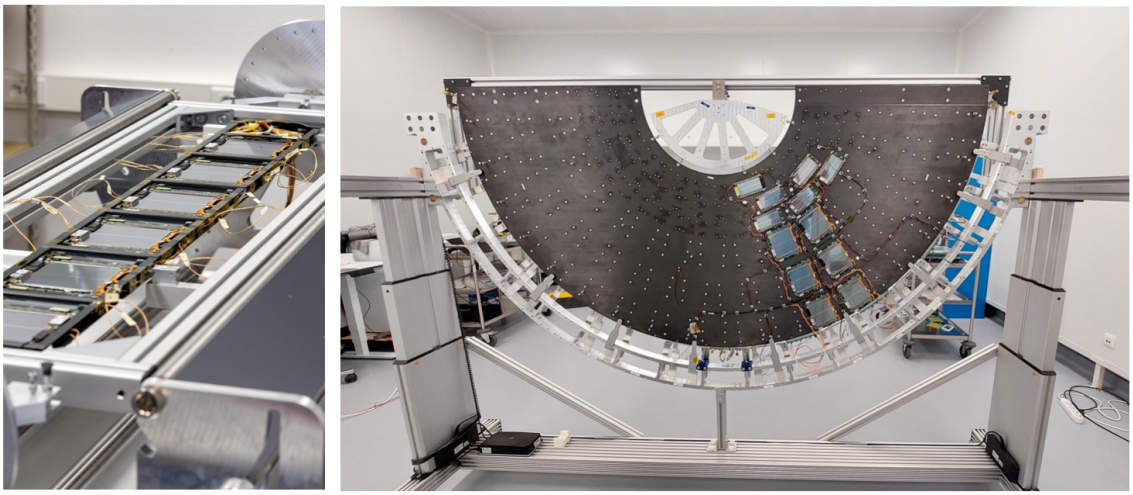

Figure 6: Fully assembled TB2S ladder (left) and TEDD dee (right).

4. Conclusions

The Phase-2 CMS tracker incorporates an innovative and challenging design featuring extended acceptance, increased granularity, and reduced material budget, key elements for operation under the challenging conditions of the High Luminosity LHC. The Inner Tracker has started the module production and through automated assembly and quality control procedures aims for high throughput production over the next three years. The Outer Tracker module production is also advancing with well-established module assembly and control processes while issues are being resolved. The module production is expected to be completed by 2027.

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