

## Electrical QC Testing of Pixel Modules in the ATLAS Inner Tracker Upgrade for the HL-LHC

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Lingxin Meng<sup>a,\*</sup> on behalf of the ATLAS ITk Collaboration

<sup>a</sup>Physics Department, Lancaster University,  
Bailrigg, Lancaster LA1 4YW, United Kingdom

E-mail: [lingxin.meng@cern.ch](mailto:lingxin.meng@cern.ch)

The upgrade Inner Tracker (ITk) for the ATLAS detector in the HL-LHC era is in its production phase. About 10000 hybrid pixel modules will be produced for the pixel detector in this all-silicon tracker. The electrical performance of these modules during quality control (QC) is assessed on the 3D and planar sensors, the RD53 frontend chip and on the module as a whole. A pixel module consists of 3 or 4 frontend chips. The interplay between the chips is derived from first principles and is evaluated during QC on the testbench. In addition to the typical leakage current measurement and chip calibration and tuning, our QC also tests the novel features of this chip that allows the radiation length of the detector to be minimised. These features include the shunt-LDO (SLDO) circuit which enables powering of multiple modules in a serial chain and on-detector data aggregation.

The assembly and testing of these modules are performed at about 25 sites worldwide, thus it is of utmost importance to ensure the consistency and uniformity of the testing procedures. For this purpose, we have developed a modular testing suite based on python that is easily installed and automates tasks like interacting with the production database, conducting tests with pre-defined procedures, interpreting the measurements and the creation of a test report.

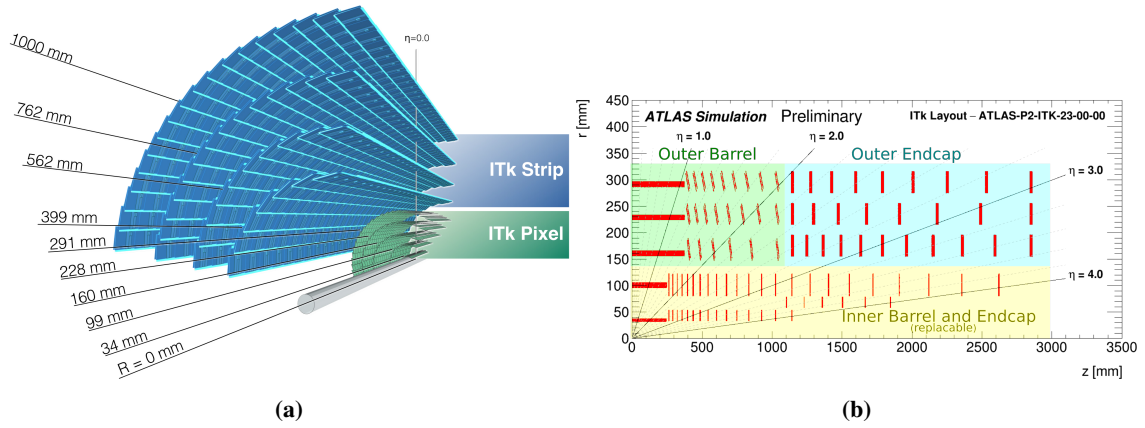
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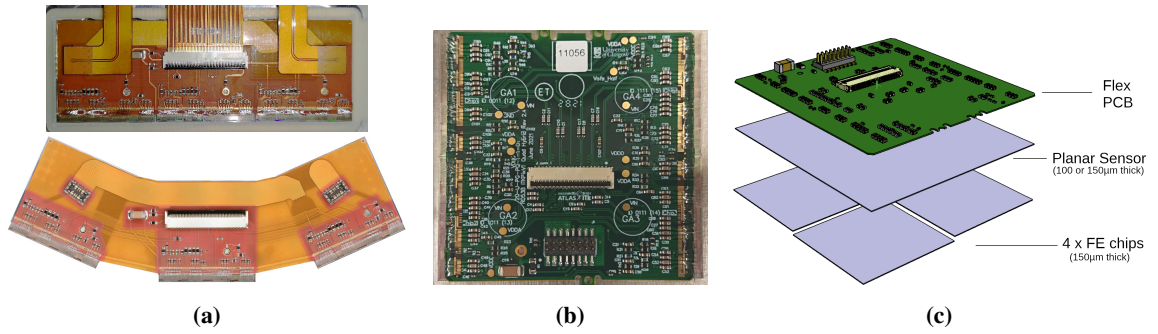
\*Speaker

## 1. Introduction

The ATLAS [1] Inner Tracker (ITk) [2] upgrade for the high-luminosity LHC era is in its production phase. This all-silicon tracker consists of a strip and a pixel subdetector as shown in figure 1a. The pixel detector [3] comprises  $13 \text{ m}^2$  silicon sensors consisting of 8372 modules with 5 billion pixels. They are distributed over 5 layers within 3 subsystems as shown in figure 1b, where the innermost layers (L1, R0 and R0.5) contain pseudo-triplet modules in different geometries as shown in figure 2a, while the outer layers contain quad modules as shown in figure 2b which make up about 95% of all modules. The components stack making up the module is shown in figure 2c for the example of a quad module which consists of a sensor tile and 4 frontend (FE) chips.



**Figure 1:** (a) Transverse view of the ITk layout. (b) Crosssection of active elements in the pixel detector. [2]



**Figure 2:** Two pixel module flavours: (a) a linear triplet (top) for the L0 barrel and a round triplet module (bottom) for the R0.5 coupled rings; (b) a common quad module. (c) Component stack of a quad module.

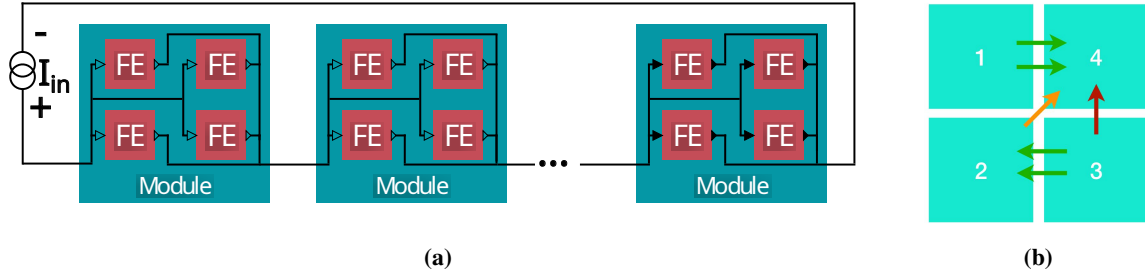
## 2. Minimisation of Material Budget

Being the heart of the ATLAS detector, it is important for tracking performance to minimise the material budget. The ITk pixel system utilises two methods: serial powering and on-module data aggregation.

Up to 14 modules on a local support are powered in series by a constant current of e.g. 6.25 A for layers 2–4, while on a module the chips are powered in parallel, as shown in figure 3a. Compared

to 14 times 6.25 A in a parallel powering scheme, serial powering minimises the amount of power cables, reduces the thermal load which further minimises the material required for cooling.

Each frontend chip is capable of  $4 \times 1.28$  Gbps data uplinks, which results in up to 16 data links on a quad module. However, for modules further away from the interaction point, the hit rate and thus the data rate can be significantly lower so that not all data links are required. Therefore, data can be aggregated on a module by routing the data of some chips to other chips and use the data merging capability of the frontend chip, as shown in figure 3b. Thus, while in the innermost layer all 4 links per chip are required on a triplet module (up to 12 links per module), in L3, data from all four chips on a quad module are merged into one single link.

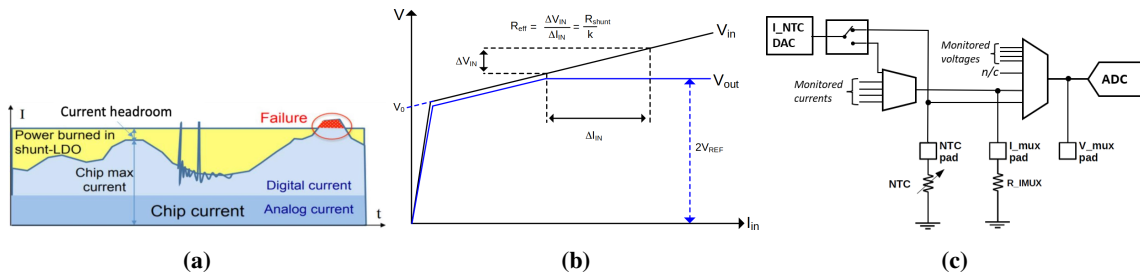


**Figure 3:** (a) Schematic for serial powering. (b) Routing of chip data lanes on a quad module.

### 3. RD53 Frontend Chip

The frontend chip used in the ITk pixel detector is the RD53 chip [4] developed for both the ATLAS and CMS inner tracker upgrade. To support the serial powering concept, the chip has implemented shunt-LDO (SLDO) voltage regulators for both the analog and digital domains. Figure 4a depicts different current consumption scenarios in 4a and an example SLDO turn-on curve in 4b. In addition, there are over-voltage and under-shunt protections, as well as a low-power operation mode for first checks during integration before the final detector cooling is permanently connected.

The chips can be identified by unique electronic fuse (eFuse) that are written during wafer probing, which encodes a chip's wafer number (WWW) and its row (R) and column (C) positions



**Figure 4:** (a) Varying current consumption of one readout chip at a constant current. (b) Example SLDO characteristics curve with the input voltage  $V_{in}$  (black) and regulator output voltage  $V_{out}$  (blue) as functions of the input current, and the offset voltage  $V_0$ . (c) Diagram of the monitoring block with current and voltage MUXes feeding the input of the ADC. [4]

on the wafer in hexadecimal 0xWWWRC format. To distinguish data from different chips during data merging and to address individual chips on a module using one commandline, a 4-bit chip ID is set via wirebonds.

Monitoring features are essential for testing and operation. Through the analog multiplexer (MUX), internal currents and voltages can be routed out for monitoring through the V\_mux pad or digitised on-chip via the 12-bit ADC as shown in figure 4c. In addition, there are 5 on-chip temperature sensors and wirebond pads for external NTC readout. Ring oscillators are implemented as indicators for radiation damage.

#### 4. Pixel Module Quality Control during Production

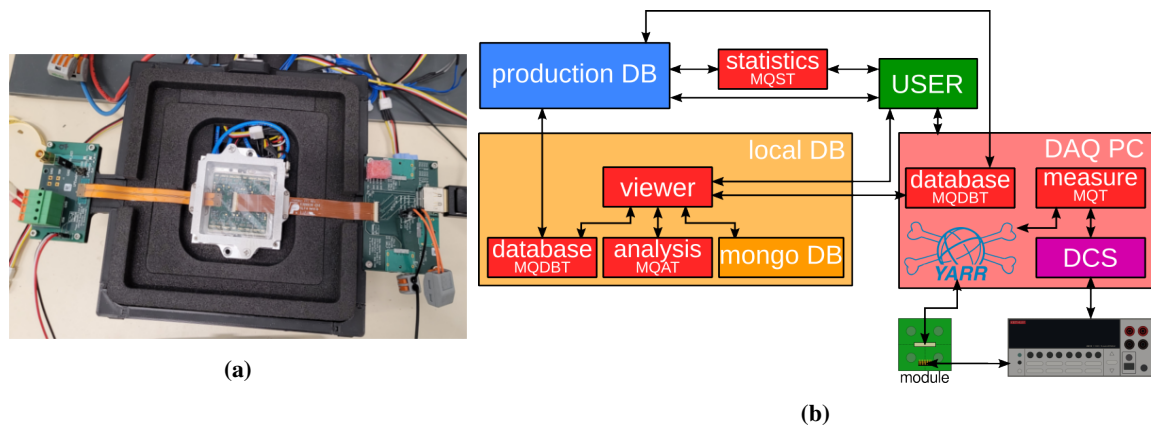
The production of about 10000 modules including yield takes place at about 25 institutes world wide. Each subcomponent undergoes QC before being assembled to a module. Then the module undergoes a number of stages, such as wirebonding, parylene coating, attachment of wirebond protection for Outer Barrel modules, thermal cycling, and shipment to loading sites. Between the stages identical tests are performed on the module. To ensure the tests are consistent between institutes and stages, many common tools are developed to be deployed by every site along with site qualification steps to be completed.

The subcomponents of modules, i.e. sensors, FE chips and module PCBs are quality-controlled before being hybridised at vendors.

##### 4.1 Module Electrical Quality Control

All parts in the QC setup in figure 5a are common developments. It consists of a cooling box containing a quad module inside a module carrier. The module is connected via data and power pigtailed to data and power adapter cards which then lead to the data acquisition (DAQ) and detector control system (DCS), respectively.

The testing procedures are documented in great details are implemented in the common module QC software. The acceptance criteria per layer applied in these tests are calculated based on chip activity and configuration, the electronics design, cooling capability and other system requirements.



**Figure 5:** (a) Testing setup with common parts [5]. (b) Interactions between common software infrastructures.



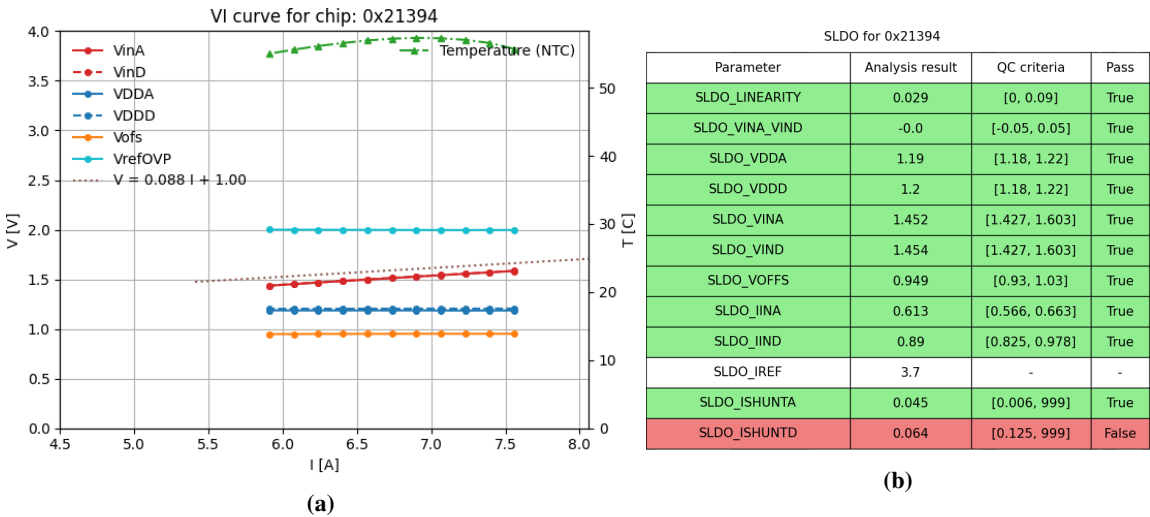
The Module QC Tools are a set of pip-installable python packages consisting of database, measurement, analysis tools and local database (LDB) viewer. They can be used stand-alone but it is intended that they interact with each other as shown in figure 5b.

Module QC database tools (MQDBT) [6] interfaces with the central ITk production database (PDB) and the LDB [9]. They are primarily used to generate chip configuration files from wafer probing results saved in the PDB. Additional functionalities include reviewing a component's stages and available tests and uploading measurements onto LDB or PDB.

The DAQ used for module QC is YARR [10] which is also used by the ITk strip project. It comprises custom software and firmware for the usage of commercial Kintex 7 FPGA boards with custom FMC card providing 4 mini DisplayPorts. The DAQ is executed by Module QC Measurement Tools (MQT) [7] to read out the module. MQT is configurable to adapt to the different hardware and software infrastructures at each module testing site. For example, a different DAQ can be used instead of YARR and DCS commands can be specified. MQT record the raw values which are then saved in the PDB to allow a re-analysis with updated software. The Module QC Analysis Tools (MQAT) [8] are the central module analysis package which contains electrical as well as non-electrical calculations and cuts to analyse the raw measurements. As python packages, MQDBT and MQAT can be imported by other tools like LDB viewer, which is a web GUI that interfaces with a local MongoDB instance to store and manage components and measurements on-site, runs analysis and uploads final results into the PDB. With these tools, the testing time per module for electrical QC tests listed in section 4.2 is about 1 hour 40 minutes without IV and source scan. The time increases accordingly if more complex software infrastructure is set up or human intervention is required.

## 4.2 Electrical QC Tests

The module electrical tests are performed in a fixed order from the most basic to more complex functionalities. The low level tests are sensor IV to full depletion and no early breakdown, core



**Figure 6:** (a) Plot of SLDO chip voltage against input module current. (b) SLDO results table with the digital shunt current being too low and thus failing the QC criteria.

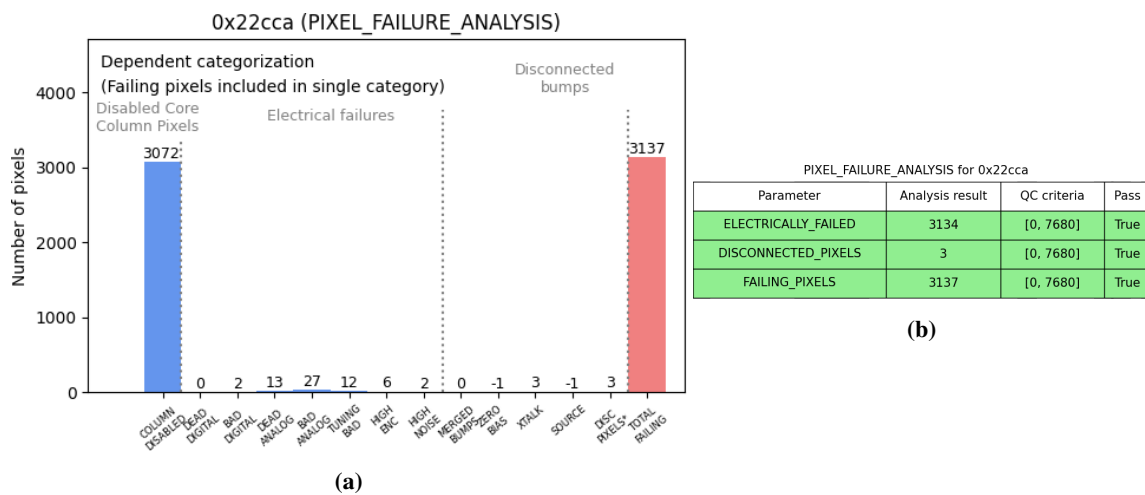
column scan to address the core column issue [11], calibration of the chip internal ADC which then can be used for subsequent tests without an external multimeter, analog register readback to verify the register reading functionality and the register value, SLDO regulator curve as shown in figure 6 to ensure serial powering, calibration of the injection circuit for pixel matrix tuning, test of low-power mode, and data transmission to test link quality and verify data merging modes.

Higher level tests contains multiple pixel matrix scans. The order of these scans are from the end of the readout chain towards the interface to the sensor.

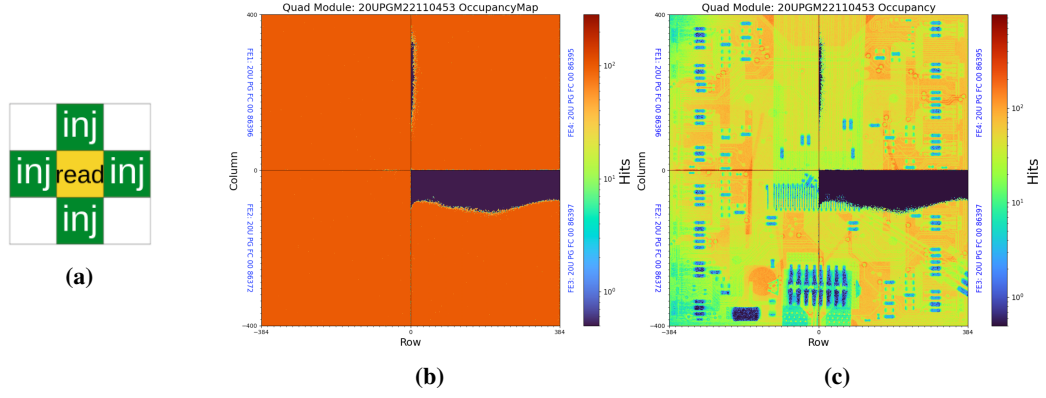
**Minimum health test** includes a minimal set of scans to provide the digital and analog performance, as well as time-over-threshold (ToT) and threshold distributions before or after tuning, depending on the stage this test is run.

**Tuning** equalises global threshold, ToT, and pixel threshold across the pixel matrix.

**Pixel failure analysis** combines digital, analog, ToT, threshold, noise and disconnected bump scans to classify the identified pixel failures of each module into an exclusive category as shown in figure 7a. The ultimate test to verify the whole readout chain is to detect signals from ionising particles. Usually, a scan with radioactive sources is performed. However, due to radiation protection and additional handling and running time, source scans are less practical and have been phased out. Instead, bump disconnection in ITk pixel module QC is determined based on crosstalk between pixels through depleted sensors. With a fully depleted planar sensor, we expect a crosstalk of about 2% of the injection charge from a direct neighbouring pixel. The crosstalk-based disconnected-bump scan utilises this mechanism and injects charge into 4 direct neighbouring pixels while reading out the central pixel as shown in figure 8a. While the overall comparability between source scan and crosstalk-based disconnected-bump scan is very good, as can be seen in figure 8, each has its advantages and disadvantages regarding the effectiveness at interfaces, with neighbouring disconnected pixels and under SMD components. However, either of the two method



**Figure 7:** (a) High to low level exclusive pixel failure classification (-1 indicates no data). (b) Numbers of electrically or mechanically (bump-bond) failed pixels, and the total number of failed pixels per chip.

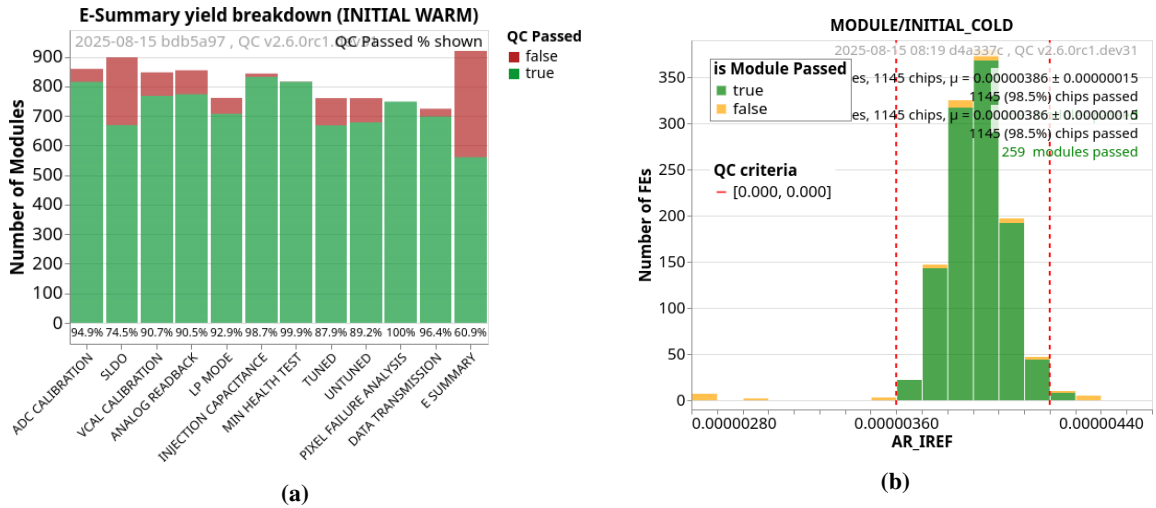


**Figure 8:** (a) A pixel and its 8 neighbours. The central pixel should detect a charge from crosstalk charge injected into its four direct neighbours. (b) Occupancy map of a quad module from a crosstalk-based disconnected bump scan. (c) Occupancy map of a quad module from an x-ray source scan.

is sufficient to reflect issues in hybridisation. The crosstalk-based method does not require any manual intervention or additional safety requirements and is as fast as an analog scan.

### 4.3 Module Data Reporting and Monitoring

To monitor data in the PDB and react timely to any systematic issues, module data reporting is in place. Breakdown plots of modules yields are available for different tests as shown in figure 9a. Currently, modules with core column issues contribute to a high failure rate in many tests. Within each test, distributions are available for all measured parameters as shown in figure 9b.



**Figure 9:** (a) A breakdown of modules passing and failing each test. (b) Distribution of a measured parameter in a test.

## 5. Summary and Outlook

We have developed a set of detailed procedures and user-friendly software that makes use of database structures and takes production flow into account. The software is modular but also interacts seamlessly with each other. The procedures and software have been verified by many module production institutes, the analysis and initial criteria derived from first principles have been verified by module data and have been updated and relaxed. All module QC tools are being used at all production sites as ITk pixel modules are in the production phase. Further optimisations are foreseen, as well as extension of functionalities to modules on local supports.

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