PROCEEDINGS OF SCIENCE

Performance of the AstroPix Prototype Module for the Barrel Imaging Calorimeter at the ePIC Detector and in Space-Based Payloads

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AstroPix is a high-voltage CMOS (HV-CMOS) monolithic active pixel sensor originally developed to enable precision gamma-ray imaging and spectroscopy in the medium-energy regime (~100 keV–100 MeV) based on the groundwork laid by ATLASpix and MuPix. It features a 500 µm pixel pitch, in-pixel amplification and digitization, and low power consumption (~3-4 mW/cm^2), making it scalable for large-area, multilayer telescope detector planes. The detectors have a designed dynamic range of 25 keV to 700 keV.

With these features, AstroPix meets the requirements of future space-based high-energy telescopes and the imaging layers of the Barrel Imaging Calorimeter (BIC) in the Electron-Proton/Ion Collider (ePIC) detector at the future Electron-Ion Collider (EIC). For the space-based payload, AstroPix is being integrated into sounding rocket and balloon payloads to demonstrate the technical readiness of the devices. For BIC, AstroPix-based imaging layers interleaved within the lead/scintillating-fiber (Pb/SciFi) sampling calorimeter provide granular shower imaging, enabling key performance features such as electron/pion or gamma/neutral pion separation.

As part of the ongoing detector R&D efforts, we have been testing various AstroPix_v3 configurations: the single chip, a quad-chip assembly, a three-layer stack of quad chips, and a 9-chip module that represents the smallest prototype unit of the BIC imaging layer. This presentation will highlight recent performance test results from these AstroPix detector configurations.

33rd International Workshop on Vertex Detectors (VERTEX2025)
25-29 August 2025
University of Tennessee, Knoxville, USA

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 ISSN 1824-8039 . Published by SISSA Medialab.

PoS(VERTEX2025)031

1. Introduction

A novel High-Voltage CMOS (HV-CMOS) monolithic active pixel sensor named AstroPix has been developed for the proposed All-sky Medium-Energy Gamma-ray Observatory eXplorer (AMEGO-X) mission concept, a medium-energy (100 keV–100 MeV) gamma-ray telescope designed to deepen our understanding of astrophysical phenomena by identifying and characterizing gamma-rays from explosions and high-energy particle acceleration in the universe [1]. The ComPair-2 balloon mission serves as a flight-like prototype for the AMEGO-X, designed to validate detector design and performance in a near-flight environment [2]. It features a 10-layer tracker with 95 quad-chips per layer and a 4-layer calorimeter composed of 24 CsI bars coupled to SiPMs on each side, as shown in Fig. 1. To further validate the tracker subsystem layers of a Compton and pair (ComPair-2) gamma-ray telescope in a relevant space-like environment, the AstroPix Sounding Rocket Technology dEmonstration Payload (A-STEP) is being developed to demonstrate a three-layer stack of AstroPix_v3 quad-chips on a sub-10 minute sub-orbital rocket flight [3].

The Electron-Ion Collider (EIC) will explore matter's inner structure to provide unprecedented 3D imaging of protons and nuclei and study gluon dynamics, including proton spin, saturation, and confinement. The EIC will provide a unique beam environment where polarized electrons collide with polarized protons and light nuclei, as well as unpolarized heavier nuclei, at asymmetric beam energies, offering center-of-mass energies of 20–140 GeV and luminosities up to 10^{34} cm^{-2}/s. The Barrel Imaging Calorimeter (BIC) is an essential component of the ePIC detector for the first EIC experiment. It serves as the barrel electromagnetic calorimeter, combining lead-scintillating fiber sampling calorimeter layers (Pb/SciFi layers) with AstroPix-based imaging layers to provide precise energy and shower profile measurements. AstroPix layers embedded in the front half of the calorimeter will provide fine-grained three-dimensional shower imaging, enabling key performance capabilities such as $e^-/\pi^\pm$ and γ/π^0 separation, which are critical for Deep Inelastic Scattering (DIS) measurements [4, 5].

As shown in Fig. 1, BIC consists of 48 sectors, each containing an AstroPix imaging layer and Pb/SciFi layers. The AstroPix layer is composed of trays, and each tray contains 72–84 modules. Therefore, the AstroPix module with a nine daisy-chained chips constitutes the basic unit of the BIC imaging layer, while the quad-chip serves as the fundamental unit for the A-STEP and ComPair-2 payloads. The present study focuses on validating the performance of these prototype modules and demonstrating their operational feasibility.

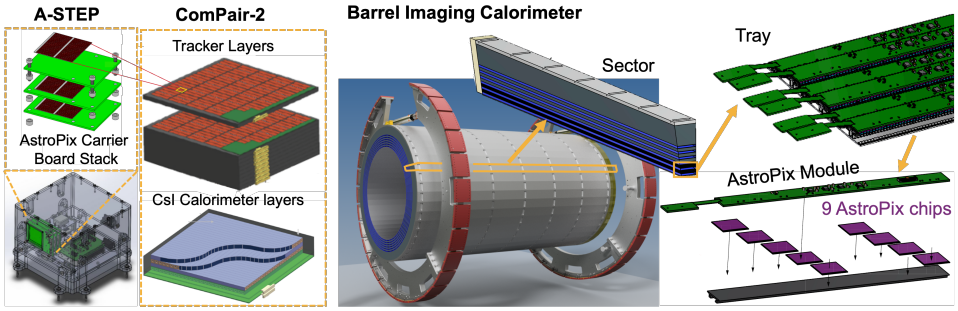


Figure 1: Detector structure of A-STEP and ComPair-2 missions at NASA Goddard Space Flight Center (left) and Barrel Imaging Calorimeter (right).

2. AstroPix_v3

Since 2019, AstroPix_v3 has been developed and tested from version 1 to version 4 [6–10]. AstroPix_v3 is the first full-size chip and has been selected for the A-STEP, ComPair-2, and BIC projects, serving as the current prototype. It has the reticle ~2×2 cm^2 size and features a 35 × 35 pixel matrix with a pixel pitch of 500 µm. AstroPix_v3 was fabricated using TSI Semiconductors' 180 nm process with a substrate resistivity of 200–400 Ω· cm and thickness of 725 µm. The design includes row and column hit buffers and supports an OR'ed rows-and-columns readout scheme. It has in-pixel amplification and low power consumption (~3–4 mW/cm^2), making it scalable for large-area, multilayer tracker telescope detector planes. The chip operates with a 2.5 MHz clock for a time of arrival (ToA) with an 8 bit counter and up to 200 MHz clock for Time-over-Threshold (ToT) measurement with a 12 bit counter. Each hit in the row/column readout generates a data packet containing the payload size, layer, chip ID, row/column number, ToA, and ToT. AstroPix_v3 employs streaming readout and self-triggering at the pixel level, where each pixel autonomously records hits above threshold.

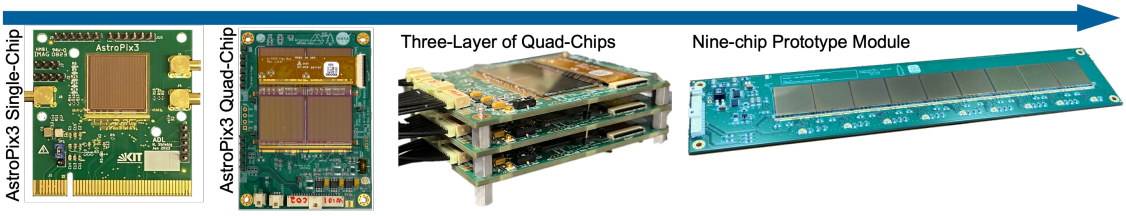


Figure 2: AstroPix_v3 configurations: stepwise progression from single-chip to nine-chip prototype module.

Starting from the single chip, each configuration has been tested with progressively increasing scale, as shown in Fig. 2. The single chip has ~2 cm × 2 cm; the quad-chip is a 2 × 2 array of single chips (sensor size ~4 cm × 4 cm); and the nine-chip module is a 1 × 9 linear array of single chips. For the single-chip module, bond pads located along the lower edge of the chip digital periphery were directly wire-bonded to a rigid carrier PCB. For the quad-chip module, the bond pads along the lower edge of the digital periphery of the top chips were wire-bonded to a flexible PCB bus bar, which was mounted on the top chips to provide power and communication. The quad-chip and nine-chip modules were subsequently connected in a daisy-chain configuration and read out via a SPI interface.

3. Test Results

The main goal of the tests with various AstroPix_v3 configurations is to validate their operation—including basic device functionality such as DAQ communication and daisy-chain readout—as well as performance aspects such as noise level, chip uniformity, pixel-to-pixel variation, and rate capability, evaluated through injection tests, cosmic-ray tests, and source tests. Based on the performance result of single-chip tests, a bias voltage of -150 V and a global threshold of 200 mV were applied to all AstroPix_v3 configurations with the current setups. The performance of the AstroPix_v3 single-chip, including noise characteristics, injection response, energy resolution, calibration, and dynamic range, has been reported in previous studies [7, 8].

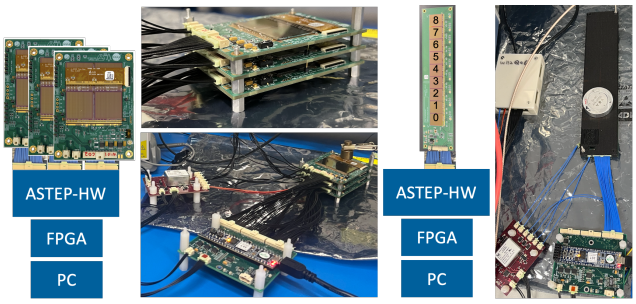


Figure 3: Pictures of the bench test setup with AstroPix_v3 configurations.

For data acquisition, the A-STEP hardware (A-STEP HW) developed as a sounding rocket payload, together with a commercial Cmod A7 Artix-7 FPGA Module, was used for the current performance evaluation, as depicted in Fig. 3. This system includes an HV bias board that supplies up to –150 V to each AstroPix_v3 carrier board and supports configurations of up to three layers of quad-chips or nine-chip modules. Testing was performed with a quad-chip, a three-layer stack of quad-chips, and a nine-chip module. In this section, representative test results with AstroPix_v3 multi-chip configurations are highlighted.

3.1 Quad-chip

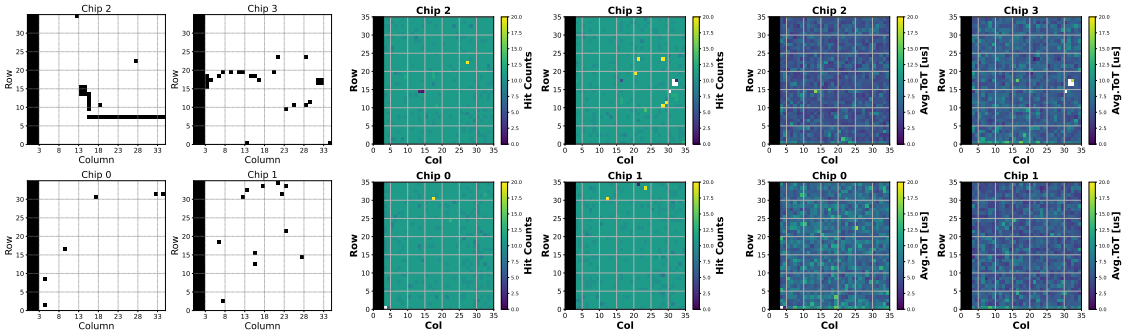


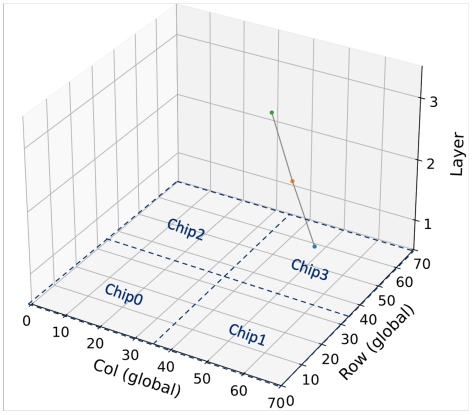
Figure 4: Mask map of the quad-chip module (left) and results of the injection test: hit map (middle) and ToT map (right). Each plot corresponds to one chip in the 2×2 array.

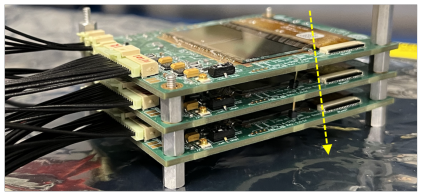
As shown in Fig. 4, the mask maps of a quad-chip were obtained by measuring noise-triggered counts per chip, and pixels with a noise rate greater than 2 Hz were masked and shown in black. The first three columns were additionally masked because they use a different comparator design, which causes larger noise due to higher amplification. An active pixel yield of 99% was achieved in the two bottom chips, while a slightly lower yield of ≥97% was observed in the two top chips due to the noise induced by a digital communication line on the flexible PCB bus bar, which appears as a straight line in chip 2 and as a curved line near the middle-right side of chip 3. This effect is present only under multi-chip activation, appearing when three or four chips are enabled simultaneously, and is not observed in per-pixel readout tests.

The injection test was performed to evaluate pixel-to-pixel response uniformity and variation, using the same injection voltage per pixel, based on the hit and ToT maps. Hit maps, presenting

the hit count per pixel, and ToT maps, presenting the average ToT value per pixel for each chip of the quad-chip, are shown in Fig. 4. Expected total counts per pixel is about 10–11 counts and hit maps shows good uniformity across the chips except for a few pixels. Some pixels did not respond properly to the injection, and a few masked pixels show abnormal hit counts. ToT maps present mean ToT values for each pixel and shows both chip uniformity and pixel-to-pixel response variation. Most pixels exhibit mean ToT values generally in the range of 5–7 µs, and their ToT distributions are well described by a Gaussian function with respect to the injection voltage. These results are comparable with AstroPix single-chip pixel-to-pixel variation of 20–30%.

3.2 Three-layer stack of quad-chips as the A-STEP payload





Layer	Chip ID	(Col, Row)	ToT [µs]
3	3	(7, 10)	6.72
2	3	(13, 10)	9.20
1	3	(19, 11)	10.08

Figure 5: Cosmic-ray event display of a three-layer stack of quad-chips (left) and hit information.

The cosmic-ray test was performed to verify the performance of a three-layer stack of uncalibrated quad-chips and to ensure the proper operation of the software and firmware under development. The system was designed to distribute a common AstroPix ToA clock across the three quad-chip layers to enable coincident measurements.

Fig. 5 shows a representative event display of a cosmic-ray trajectory reconstructed from a coincident event in which all three layers recorded the same AstroPix ToA within one tick, corresponding to 400 ns. In the figure, the top-right panel shows the three-layer quad-chip configuration, and the bottom-right table presents the corresponding hit information. Since the chips have not yet been calibrated, the ToT values were not considered in the analysis.

The chips in each quad-chip module are daisy-chained such that data from chip 3 is sequentially transmitted to chip 0 and then forwarded to the FPGA. As the three quad-chip layers operate simultaneously, this demonstrates successful readout of 12 chips in total. These results confirm reliable system communication and validate the capability of the prototype A-STEP detector to operate multiple daisy-chain configurations with shared timing information.

3.3 Nine-chip prototype module as a unit of the BIC imaging layer

The noise scan for the nine-chip prototype module was performed in the same way as for the quad-chip test, and the resulting mask maps for each chip are shown in Fig. 6, similar to those in Fig. 4. In the nine-chip module, a tighter noise-rate cut of 1 Hz was applied, compared to 2 Hz

for the quad-chip module. The current prototype achieved a 99% active pixel yield for all chips except the last chip, which had 91 noisy pixels corresponding to a 91.9% active pixel yield. In pre-production, only chips that pass quality control with more than 99% good pixels will be used.

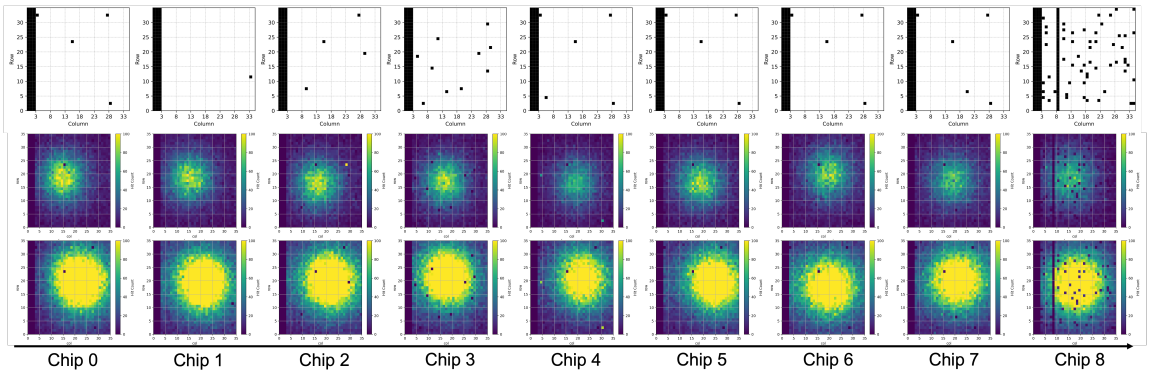


Figure 6: Mask map of the nine-chip module (top) and hit maps from the ^{90}Sr source test with the nine-chip module using 3 mm (middle) and 5 mm collimators (bottom).

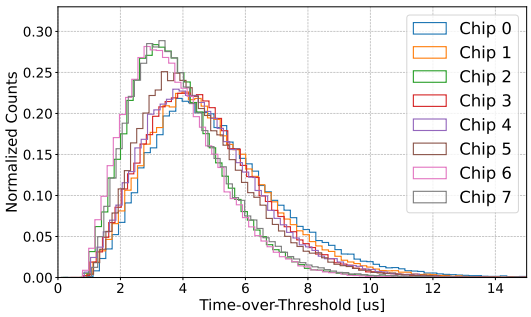


Figure 7: ToT distributions from the ^{90}Sr source test with the nine-chip module

Using this module, a source test was subsequently conducted. A 10 µCi ^{90}Sr source was manually moved to the next chip every 1 minute. Fig. 6 shows hit maps for each chip obtained with 3 and 5 mm diameter collimators, where black pixels indicate masked pixels. The hit maps exhibit good alignment with the source position, with a larger number of responsive pixels and higher hit counts observed for the larger-diameter collimator.

The normalized ToT distributions for chips 0–7, excluding chip 8, are presented in Fig. 7, obtained from the ^{90}Sr source measurement using a 5 mm diameter collimator. They are well described by a Landau function convoluted with a Gaussian function. Each distribution includes all pixels within the corresponding chip and reflects its average response characteristics. The nine-chip module exhibits two distinct ToT response groups: one comprising chip 2, 6, and 7, which show a relatively lower ToT response with a most probable value around 3 µs, and another including chip 0, 1, 3, 4, and 5, which exhibit a slightly higher ToT response with a most probable value around 4 µs. In addition, consistent ToT distributions were observed regardless of the collimator size, and the distributions are comparable to those measured in the single-chip tests. These results demonstrate that the nine-chip prototype module operated as intended with the current setup, including daisy-chained readout.

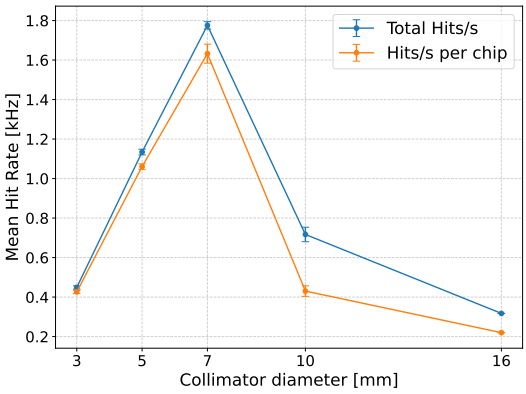


Figure 8: Mean hit rates per nine-chip module and per chip measured in the ^{90}Sr source test.

With the same setup, a hit rate measurement was performed to validate the readout capability of the nine-chip module and to measure the maximum achievable hit rate. A 10 µCi ^{90}Sr source with different collimators was placed above chip 1, which had only one masked pixel. The hit rate, defined as the number of recorded hits divided by the data-taking time, was measured five times for each point, and the mean values and standard deviations were plotted in Figure 8. The figure shows the mean hit rates as a function of collimator size, with the total and per-chip rates indicated in blue and orange, respectively. The maximum per-chip rate was measured to be about 1.6 kHz, and reliable operation was maintained up to a collimator diameter of 7 mm, beyond which significant data dropout were observed with the current setup.

The maximum expected hit rate per chip for the imaging layers in the EIC environment is about 925 Hz, taking into account DIS, electron, and proton beam backgrounds. For space-mission conditions, the expected hit rate of the A-STEP detector is approximately 1 Hz/cm^2, and under the assumption of a very bright GRB simulation, it increases to about 45 Hz per chip for AMEGO-X. Under the current setup, the nine-chip prototype module satisfies the requirements for both the BIC imaging layers and A-STEP.

4. Summary

Several AstroPix_v3 configurations, including the quad-chip and nine-chip prototype modules, were successfully tested. The quad-chip achieved reliable readout and a three-layer stack demonstrated synchronized multi-layer operation, confirming the scalability of the design. The nine-chip prototype also achieved a 99% active-pixel yield with stable performance and satisfied the hit-rate requirements, indicating reliable operation under realistic beam conditions. The measured performance meets the requirements for both the BIC imaging layers at the EIC and the A-STEP space mission. Although the hit-rate test was conducted with the nine-chip prototype, the results confirm sufficient performance for the quad-chip detector planned for A-STEP. Overall, the AstroPix_v3 design proves feasible for both collider and space-based detector applications, while the current design is limited to to a maximum hit rate of approximately 4 Hz per pixel. Future versions are under development to achieve substantially higher hit rates at both the pixel and chip levels, along with full depletion, fast time resolution, and low power consumption.

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