PROCEEDINGS OF SCIENCE

Monolithic active pixel sensors based on the TPSCo 65 nm imaging CMOS technology: an overview of results and future challenges

Giacomo Ripamonti[a]*

[a] *CERN,*
Esplanade des Particules, 1, 1217 Meyrin, Switzerland

E-mail: giacomo.ripamonti@cern.ch

Monolithic active pixel sensors (MAPS) are a key enabling technology for the next generation of detectors in High-Energy Physics experiments due to their low material budget, fine spatial resolution, and scalability to large areas at low cost. Building on the success of ALPIDE in the ALICE ITS2 detector, the CERN EP R&D program in synergy with the ALICE experiment have adopted the TPSCo 65 nm imaging CMOS process to address the demands of future detectors. This technology node enables smaller pixel pitches, increased output data rates and radiation hardness compared to the 180 nm technology adopted for ALPIDE, and allows the design of wafer-scale sensors through the stitching technique.

This paper presents the evolution of the R&D program from initial technology qualification with small-area prototypes to the development of the wafer-scale stitched sensor prototypes MOSS and MOST, and the full-size, full-functionality wafer-scale MOSAIX prototype for the ALICE ITS3 vertex detector. Building on the results obtained for MOSS and MOST, MOSAIX integrates 9.97 million pixels with on-chip high-speed data links and advanced power segmentation, resulting in an unprecedented level of integration and complexity in the high energy physics community. In parallel, the Hybrid-to-Monolithic (H2M) ASIC demonstrates the feasibility of embedding hybrid pixel detector functionalities in a monolithic sensor. The paper also outlines future challenges for upcoming detectors such as ALICE3 and FCC-ee, including further pixel pitch reduction, increased speed of the front-end for the same power consumption, further minimization of the inactive area, and enhanced radiation tolerance.

33rd International Workshop on Vertex Detectors (VERTEX2025)
25-29 August 2025
University of Tennessee, Knoxville, USA

*The presented work has been performed in the context of the CERN EP R&D program (primarily within the Work Package 1.2 on monolithic sensors), in synergy with the ALICE collaboration.

ISSN 1824-8039. Published by SISSA Medialab. https://pos.sissa.it/

PoS(VERTEX2025)034

1. Introduction

Monolithic active pixel sensors (MAPS) are crucial for current and future High Energy Physics (HEP) detectors, due to their minimal material budget, low power consumption and low cost per unit area. Following the successful deployment of the first detector based on MAPS at CERN (ALICE Inner Tracker System 2, ITS2) adopting the ALPIDE ASIC designed in the TowerJazz 180 nm imaging CMOS technology [1–3], the investigation of the TPSCo 65 nm imaging technology was started. This effort is done in the framework of the CERN Experimental Physics (EP) R&D program, in synergy with the ALICE experiment, interested in developing a wafer-scale, stitched sensor for its ITS3 upgrade to replace the inner layers of the ITS2. The smaller feature size of this 65 nm technology is crucial to match the requirements of pixel pitch, output data rate and radiation hardness of future HEP detectors. In addition, this technology allows the fabrication of wafer-scale sensors on larger wafers (300 mm instead of 200 mm for the 180 nm process) enabling the reduction of the material budget to less than 0.09% X_0, due to the inclusion of all power and data connections on chip.

The R&D effort presented in this work has the goals of designing a wafer-scale stitched sensor for application in ALICE ITS3, of investigating new concepts for CMOS sensors (like porting the hybrid pixel detector architecture into monolithic), of optimizing the performance of MAPS achieving improved timing, reduced power consumption and increased radiation tolerance. Within the context of the CERN EP R&D program, access and support in the HEP community to the TPSCo 65 nm imaging technology is also provided.

This article provides an overview of this R&D program, highlighting the path from the design and characterization of test structures to qualify the technology for use in HEP, to the development of wafer-scale sensors.

2. Initial activities on the TPSCo 65 nm imaging technology

Several 1.5 mm x 1.5 mm chips have been initially prototyped with the goal of developing knowledge about the technology, of characterizing pixels, transistors and building blocks for MAPS. These ASICs allowed to demonstrate fully efficient sensor, analog front-end, digital readout chain before and after irradiation (up to 10^{15} 1 MeV $\frac{n_{eq}}{cm^2}$ at room temperature [4]) for pixel pitches between 10 and 25 µm, and time resolution down to ≈ 65 ps from the sensor (after time walk corrections) was obtained for a 10 µm pitch [5, 6]. These results demonstrated the suitability of the TPSCo 65 nm imaging technology for HEP applications.

3. First stitched wafer-scale MAPS prototypes: MOSS and MOST

Building on the results described in Section 2, wafer-scale prototypes were designed. The stitching technique allows to fabricate chips that are larger than the reticle size and was adopted to design the Monolithic Stitched Sensor (MOSS) and the Monolithic Stitched Sensor with Timing (MOST) (the wafer hosting MOSS and MOST is shown in Fig. 1). MOSS and MOST were prototyped to learn about the stitching technique, and to study yield and uniformity of wafer-scale sensors.

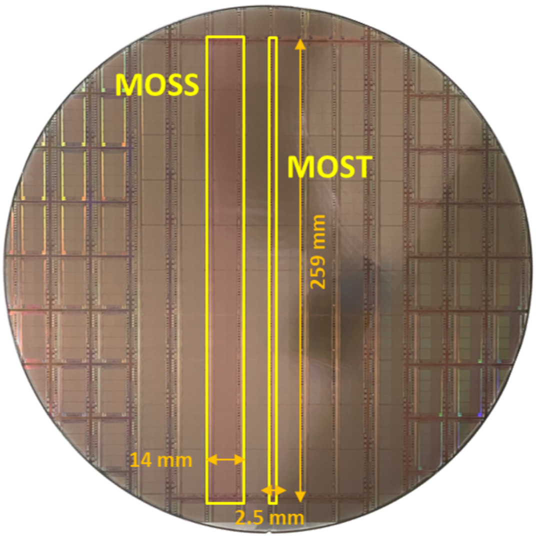

Figure 1: Picture of the wafer hosting the MOSS and MOST stitched sensors.

MOSS [7–9] is a 14 mm x 259 mm ASIC and it hosts 6.72 Mpixels, read out in a synchronous manner. Its layout is conservatively designed and two pixel pitches (22.5 µm and 18 µm) are included to investigate the effect of layout density on yield. The ASIC is constituted of:

- a Left Endcap (LEC), which allows to provide power, control and read data from the short edge of the chip (which is a requirement of ALICE ITS3),
- ten Repeated Sensor Units (RSUs). The RSUs host the pixel matrices and each can powered, read out and controlled independently,
- a Right Endcap (REC), allowing to provide power also from the short edge located at the opposite end of MOSS.

LEC, RSUs and REC are respectively highlighted in red, green and blue in Fig. 2.

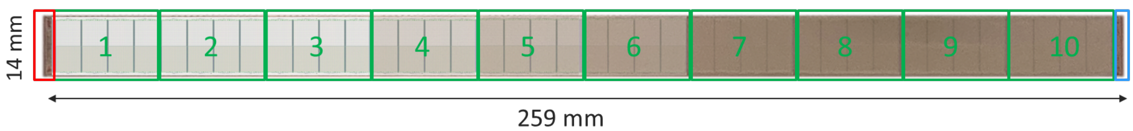

Figure 2: Picture of the MOSS ASIC, where the Left Endcap is highlighted in red, the ten Repeated Sensor Units are shown in green, while the Right Endcap is highlighted in blue.

MOSS has proven to be fully functional, and to meet the ITS3 requirements in terms of efficiency and fake-hit rate, also after irradiation (the radiation load estimated for ITS3 is $\approx$ 400 krad, $\approx$ 4 x 10^{12} 1 MeV $\frac{n_{eq}}{cm^2}$) [7, 8]. The testing campaign uncovered non-uniformities on the matrix and couplings from digital to analog circuits that led to guidelines for the design of the following prototype [10].

MOST uses instead a 18 µm pixel pitch and its size is 259 mm x 2.5 mm. Different strategies have been used in this ASIC compared to MOSS [11], in particular:

- the circuit layout is densely designed and a global power distribution network is used. Power switches are distributed across the chip to allow portions of the circuit to be connected to the global power network, and disconnected from it in case of faults. It has been demonstrated in the testing campaign that if the global power network is intact, pixel yield exceeded 99.98%, indicating feasibility for dense, large area architectures.

- An asynchronous, hit driven readout is introduced. As soon as a pixel is hit, its address is directly shipped through a 1 Gb/s global data line to the column encoders placed at the short edge of the stitched chip. The column encoders append the column address, and the data are shipped out through a CML driver. The testing of this readout mechanism allows to investigate timing preservation along global data lines on a wafer-scale stitched chip.

- Reverse bias is applied to the sensor via the front-end. In this way, the circuit ground can be tied to the substrate, which brings some advantages in the design [11].

4. MOSAIX: the full-scale, full-functionality prototype for ALICE ITS3

Following the validation of MOSS and MOST, the Monolithic Stitched Active pIXel ASIC (MOSAIX) was designed and submitted for fabrication. It is the full-scale, full-functionality prototype for ALICE ITS3 [16, 17]. MOSAIX hosts 9.97 million 22.8 µm x 20.8 µm pixels. It inherits some its features from MOSS (synchronous read-out, conservative layout) and some from MOST (power segmentation, data transmission on chip). MOSAIX is composed of a Left Endcap, twelve Repeated Sensor Units, and a Right Endcap, which have a similar role as in MOSS. Nevertheless, significant additional complexity is added to MOSAIX compared to MOSS: in particular, the LEC includes eight 10.24 Gb/s serializers to ship the data off chip, while it also hosts a 12-bit monitoring ADC to allow the measurements of relevant parameters of all the pixel matrices across the stitched ASIC. Each RSU is split into twelve tiles, and each tile (corresponding to 0.7% of the full sensor area) can be disconnected through power switches in case it shows incorrect behavior due to a fabrication defect. In addition, each of the twelve tiles features a different combination of variants of the analog front-end and of its biasing circuitry. Extensive studies have aimed at finding the optimal doping profiles for the sensors, trying in particular to minimize the sensor capacitance (for maximum signal-over-noise ratio) and the charge collection time (to maximize the efficiency after irradiation) [12]. As a result of these studies, three process variants using different doping profiles for the sensors are being prototyped. The testing campaign will aim at identifying the best combination of sensor, analog front-end and biasing circuit for application in ITS3, and a final chip adopting only the optimal combination will be produced for application in the detector. The data are sent from the pixel matrices to the LEC via a differential low-swing 160 Mb/s on-chip data transmission circuit: the differential transmission allows the data lines to be placed on top of the pixels with minimal perturbation of the analog front-end, while the low-swing operation is needed to minimize the power consumption. Including approximately three billion transistors, MOSAIX features an unprecedented level of integration and complexity in the HEP community. MOSAIX has been released for fabrication, and future publications will present the measured performances of this ASIC.

5. The H2M ASIC: porting the architecture of a hybrid pixel the detector into a monolithic chip

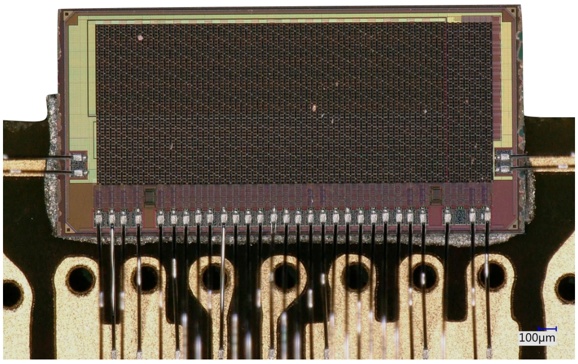

Figure 3: Picture of the H2M ASIC.

In the context of CERN EP R&D program and in collaboration with DESY and IFAE, the Hybrid to Monolithic (H2M) ASIC (whose picture is shown in Fig. 3) has been also prototyped. H2M is a technology demonstrator that aims at porting the architecture of a hybrid pixel detector into a monolithic chip [13, 14]. It includes a 64 x 16 pixel matrix with a pixel pitch of 35 µm. The larger pixel pitch compared to MOSS, MOST and MOSAIX is justified by the presence of additional circuitry per pixel, which adds to each pixel functionalities typically used in hybrid pixel detectors. In particular, four non-simultaneous acquisition modes are implemented, which respectively allow to obtain: a 8-bit Time-over-Threshold (ToT) measurement, a 8-bit Time-of-Arrival (ToA) measurement, the number of hits during the acquisition window (counting), while finally the “triggered” mode allows to use an external trigger and compensates for its fixed latency. The latter enables a shorter shutter duration compared to ToT and ToA modes, reducing the probability of noise hits [13].

The H2M ASIC demonstrated fully efficient operation, while additional work is needed to improve the fake hit rate. While the original chip thickness is about 50 µm, the die has been further thinned down to 21 µm, showing no performance degradation: this results paves the way for a further reduction in material budget in future HEP detectors. The thickness of the epitaxial layer where the signal is generated is in the order of 10 µm, is significantly lower than the pixel pitch and thus leads to mostly single-pixel clusters, limiting the spatial resolution to $\approx \frac{\text{pixel pitch}}{\sqrt{12}}$. The time resolution of H2M is limited by the non-uniform charge collection across the pixel [13]: the measured collection time is larger (while the efficiency is lower) in some regions of the pixel correlated with the n-wells layout. Such non-uniformity can be mitigated by adjusting the sensor and analog front-end parameters (in particular by employing a larger sensor bias voltage, by lowering the front-end threshold and by using a lower reset current of the charge-sensitive amplifier). This effect shed light on the challenges of designing efficient monolithic pixels with a relatively large pixel pitch and a small collection electrode. In addition, the investigations to understand such effect

PoS(VERTEX2025)034

led to the development of new simulation strategies combining TCAD, Monte Carlo and Spice simulations for future developments [15].

6. Outlook: towards ALICE3 and FCC-ee detectors

MAPS are foreseen to be adopted in future HEP detectors, such as ALICE3 [18] and FCC-ee [19] detectors. Their requirements will drive the R&D for future monolithic detectors. As an example, the main design challenges for application in the vertex detector of ALICE3 are the following [18]:

- pixel pitch of 10 µm (leading to a pixel area < ¼ compared to MOSAIX),
- power density < 70 mW/mm^2 (in MOSAIX it is < 40 mW/^{2}, nevertheless the target power density for ALICE3 is challenging to achieve, due to the significantly reduced pixel pitch and the significantly increased hit rate for the inner layers),
- $\approx$ 1 MHz/mm^2 particle hit rate,
- time resolution < 100 ns RMS,
- radiation tolerance to 300 Mrad and 10^{16} 1 MeV $\frac{n_{eq}}{cm^2}$ (while MOSAIX must tolerate 400 krad and $4 \cdot 10^{12}$ 1 MeV $\frac{n_{eq}}{cm^2}$),
- further minimization of the inactive area (which is 7% in MOSAIX).

In order to meet these requirements, several R&D activities have started. First, a sensor optimized for a pixel pitch of 10 µm has been designed and released for fabrication. In addition, front-end circuits that achieve improved speed for the same power compared to MOSAIX and fit in a 10 µm x 5 µm area including the collection electrode are in development. Readout architectures that minimize the power consumption need also to be studied. Finally, strategies to embed a large portion of the biasing circuit for the analog front-end and of the readout circuitry in the pixel matrix to minimize the dead area must be devised.

7. Conclusion

This work has presented an overview of the activities of the CERN EP R&D program on MAPS using the TPSCo 65 nm imaging CMOS technology, highlighting its role as a key enabler for future HEP detectors. Most of the presented work has been carried out in synergy with the ALICE experiment, in view of the upgrade of its vertex detector, ITS3. The small-area prototypes developed in the context of the initial technology qualification demonstrated $\approx$ 65 ps sensor time resolution and radiation tolerance up to 10^{15} 1 MeV $\frac{n_{eq}}{cm^2}$.

Building on these results, the first wafer-scale stitched prototypes, MOSS and MOST, validated the feasibility of large-area monolithic sensors, achieving full functionality and demonstrating high pixel yield as well as functioning readout architectures (synchronous for MOSS and asynchronous for MOST). These milestones paved the way for MOSAIX, the full-size and full-functionality prototype for ALICE ITS3, integrating nearly 10 million pixels, 10.24 Gb/s serializers, a low-swing differential 160 Gb/s on-chip data transmission circuit and power segmentation, representing an unprecedented level of complexity and integration in HEP MAPS developments.

In parallel, the H2M ASIC has explored porting hybrid pixel detector functionalities into a monolithic implementation, confirming efficient operation while identifying key design challenges related to timing and charge collection uniformity. These insights are instrumental for the design of future detectors.

Looking ahead, the stringent requirements of experiments such as ALICE3 and those at FCC-ee are driving further R&D efforts on smaller pixel pitches, higher radiation tolerance, faster front-end electronics, and minimal dead areas. These activities aim to push MAPS performance well beyond the current state of the art.

Finally, within the context of the CERN EP R&D program, access to and support for the TPSCo 65 nm imaging technology to the HEP community is provided, enabling broad participation in the development of next-generation detectors and fostering collaborative progress across experiments and institutes.

References

[1] M. Mager et al., ALPIDE, *The Monolithic Active Pixel Sensor for the ALICE ITS upgrade*, Nucl. Instrum. Meth. A 824 (2016) 434–438.

[2] G. Aglieri Rinella et al., *The ALPIDE pixel sensor chip for the ALICE ITS upgrade*, Nucl. Instrum. Meth. A 845 (2017) 583–587.

[3] M. Šuljić et al., *ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade*, Journal of Instrumentation 11 C11025 (2016).

[4] G. Aglieri Rinella et al., *Digital pixel test structures implemented in a 65 nm CMOS process*, Nucl. Instrum. Meth. A 1056 (2023) 168589.

[5] G. Aglieri Rinella et al., *Characterization of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process*, Nucl. Instrum. Meth. A 1069 (2024) 169896.

[6] G. Aglieri Rinella et al., *Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process*, Nucl. Instrum. Meth. A 1070 (2025) 170034.

[7] L. Terlizzi et al., *Characterization of MOSS for the ALICE ITS3 for the LHC Run 4*, Journal of Instrumentation 20 C06041 (2025).

[8] O. Abdelrahman et al., *Characterisation of the first wafer-scale prototype for the ALICE ITS3 upgrade: the monolithic stitched sensor (MOSS)*, arXiv:2510.11463 (2025).

[9] P. Vicente Leitao et al., *Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking system*, Journal of Instrumentation 18 C01044 (2023).

[10] S. Emiliani et al., *Investigation of non-idealities of pulsing circuitry in the ALICE ITS3 MOSS monolithic sensor*, Journal of Instrumentation 19 C12021 (2024).

[11] M. Selina et al., *Exploring unique design features of the Monolithic Stitched Sensor with Timing (MOST): yield, powering, timing, and sensor reverse bias*, Journal of Instrumentation 20 C07032 (2025).

[12] G. Borghello et al., *Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations* , Journal of Instrumentation 20 C07053 (2025).

[13] S. Ruiz Daza et al., *The H2M Monolithic Active Pixel Sensor — characterizing non-uniform in-pixel response in a 65 nm CMOS imaging technology*, Journal of Instrumentation 20 C06037 (2025).

[14] R. Ballabriga et al., *Characterization of the H2M Monolithic CMOS Sensor*, submitted to NIM-A, 2025.

[15] C. Lemoine et al., *Impact of the circuit layout on the charge collection in a monolithic pixel sensor*, Journal of Instrumentation 20 C06052 (2025)

[16] P. Vicente Leitao, *Development of the MOSAIX chip for the ALICE ITS3 upgrade*, Journal of Instrumentation 20 C06001 (2025).

[17] S. Bugiel, *Power distribution over the wafer-scale monolithic pixel detector — MOSAIX for ALICE ITS3*, Journal of Instrumentation 20 C02015 (2025).

[18] ALICE Collaboration, *Letter of intent for ALICE 3: A next-generation heavy-ion experiment at the LHC*, arXiv:2211.02491 (2022).

[19] A. Ilg et al., *The vertexing challenge at FCC-ee*, Journal of Instrumentation 20 C06069 (2025).

PoS(VERTEX2025)034