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Bare Module Testing for the CMS Vertex Detector Upgrade

Jesse Harris[a,*], **for the Tracker Group of the CMS collaboration.**

[a] *Department of Physics, University of Tennessee,*
1408 Circle Drive, Knoxville, USA

E-mail: jdharr218@vols.utk.edu

The High-Luminosity LHC will continue exploring physics beyond the standard model with proton-proton collisions at ten times the luminosity of previous LHC runs. The physics program depends on precise measurements of charged particles near the beams. The CMS experiment will use layers of high-granularity hybrid silicon pixel detectors. Pixelation is achieved by bonding silicon to tiny electrodes, which are directly connected to the specially designed integrated circuit, CROCv2. Pixel detector components are in the pre-production phase, and evaluating prototypes of sensor-chip assemblies from different vendors provides quick feedback and improves reliability during production. This article presents the efforts to test the viability of bare detector assemblies using a manual probe station and electronic charge-injection methods.

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*Speaker

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1. Introduction

The High Luminosity LHC (HL-LHC) will collide protons at a center-of-mass energy of 14 TeV and increase the peak instantaneous luminosity to 7.5×10^{34} cm^{-2} s^{-1}, with an average number of pileup interactions up to 200 [1]. The CMS experiment [2, 3] requires detector upgrades to handle higher particle rates [4]. The silicon pixel detector tracks charged particles closest to the proton beams, where radiation levels are highest. This new Inner Tracker (IT) will feature smaller, high-granularity pixels (size 50×50 μm^2 or 25×100 μm^2) to reduce the hit occupancy to less than 0.1% and improve spatial resolution. It also uses a serial powering scheme to minimize material, and extends its tracking coverage to $|\eta| < 4$. It consists of four barrel layers (TBPX), eight small disks (TFPX), and four large disks (TEPX) on each side, covering an area of 5 m^2 with 3900 hybrid pixel modules that have approximately 2 billion readout channels [1].

Hybrid pixel modules consist of readout chips (ROC) bump-bonded onto the 150 μm thick silicon sensor, with either two (type 1×2) or four (type 2×2) ROCs on one sensor. The CMS Readout Chip (CROC) is a 65 nm CMOS ASIC developed by the RD53 Collaboration [5], to withstand the expected hadron fluences and total ionising dose at the innermost layer of 3.5×10^{16} n_{eq}/cm^2 and 1.9 Grad, respectively [6]. The CROC features 432×336 pixels (cell size 50×50 μm^2) in a total area of 2.2×1.9 cm^2, a linear front-end with adjustable threshold (operation standard below $\sim$ 1000 e$^-$), and a high data rate (one 160 Mb/s input link and up to four 1.28 Gb/s output links). The CROC operates at a low voltage (about 1.2 V) and, therefore, requires substantial current (around 2 A per chip) due to CMOS technology. The total power consumption of the IT is approximately 50 kW. Therefore, operating the modules at low temperatures around -30° C to mitigate radiation damage to sensors and chips, as well as to minimize leakage current in the sensors, necessitates significant cooling. Maintaining consistent charge collection efficiency after irradiation requires a high bias voltage of up to 1 kV. To prevent sparks due to the high voltage near the CROC, both components are parylene-coated [7].

2. Why Bare Module Testing?

Each of the 145,152 pixels per CROC requires a reliable connection, with either two or four CROCs sharing one sensor. During the flip-chip bump bonding process, heat and force are applied to the chip. The high temperatures soften the metallic bumps on the chip, while the force presses them against the sensor pads. The small bump size of $5 - 10$ μm and large sensor sizes increase the difficulty of achieving uniform compression. Common failures include: open bumps (no signal), damaged pixels, merged bumps (short circuits), and breakthrough currents [8]. Testing of hybrid modules directly after bump-bonding is essential for spotting and fixing defects that would be hard or impossible to correct later, thereby saving time and resources in assembling the large number of modules. It provides fast feedback to manufacturers while optimizing their production process. During the Phase 1 upgrade of the ATLAS detector, the initial production batches suffered from a very high bump-bonding failure rate, as determined during threshold and noise measurements. Production was halted until the problem was solved [9]. The CMS early Phase 1 upgrade production experienced a low yield. It was found that abrasive blade dicing debris was damaging ROCs. It was decided to perform optical inspections and testing of bare modules, providing feedback to

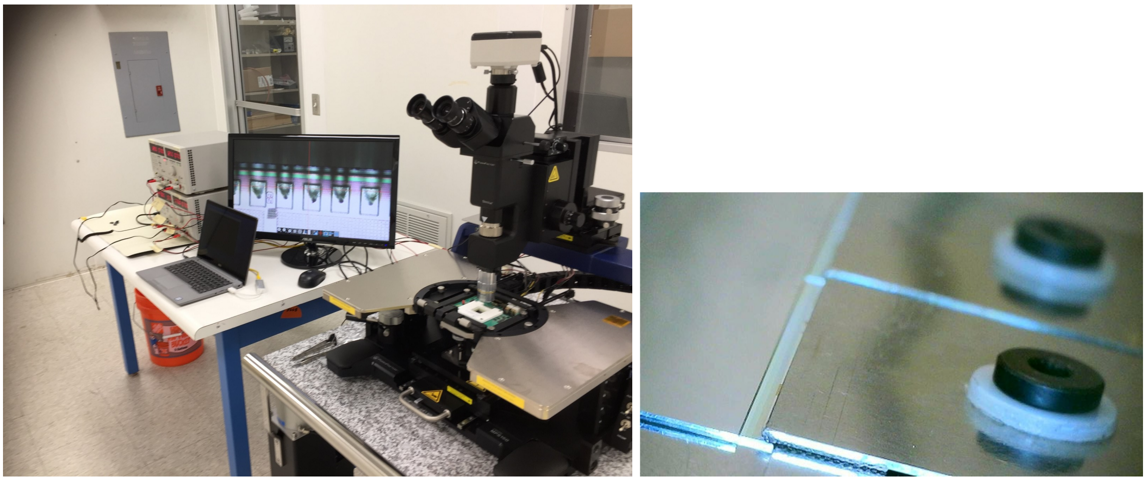

Figure 1: Left: The manual probe station (foreground) inside the cleanroom. The monitor shows a zoomed-in view of the wirebond pads from the attached camera, with needles from the probe card casting shadows. Right: Close-up of the grounding plate with the flaps attached to the wirebond pads of a 1x2 type module.

vendors, which ultimately achieved a yield above 90 % [10]. During the preproduction phase of ATLAS pixel modules for the HL-LHC upgrade, recurring chip malfunctions were observed during electrical testing. This issue could be bypassed by disabling specific pixel core columns in the readout chip. Mechanical damage to the thin modules could be a cause [11].

3. Method

Bare module testing involves several steps, including optical inspection, assessing the current-voltage (I-V) characteristic of the sensor, and conducting charge injection tests of readout chips using a needle probe card to verify the basic functionality and the quality of the pixel sensor-chip bump-bonds. The CROC chip's front-end electronics can inject a known amount of electrical charge into each pixel's preamplifier circuit, mimicking the signal produced by a real particle passing through the silicon sensor. Measurements are conducted in a clean room using an MPS 150 FormFactor manual probe station, shown in Fig. 1. It is equipped with a needle probe card [12] that contacts the 198 wirebond pads of the CROC. An Aim-TTi QL355TP device supplies digital and analog low voltages. A Keithley 2410 source meter delivers the bias voltage through a needle probe contacting the sensor's backplane.

The FPGA-based FC7 system [13] is used for data acquisition and control of the CROC, managed via the Ph2_ACF software [14], which is operated with a custom GUI that also handles the power supplies. The GUI automates a series of tuning procedures that optimize chip parameters for stable performance and perform bump-bond quality scans. By combining these features into a single, easy-to-access platform, the tool greatly enhances the efficiency and reliability of bare module testing while lowering the chance of operator errors. Overall, the process takes about 25 minutes per readout chip. The software is installed on an Alma Linux laptop.

All supply and communication cables are wrapped in aluminum foil to enhance electrical interference shielding and are connected to a common ground that includes the probe card. Since

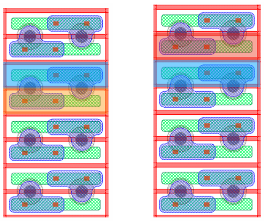

Figure 2: Crosstalk-based bump bond classification. Left: Charge is injected into the third pixel from the top (blue) and read out from the **coupled** fourth (orange). Right: In the **uncoupled** case, the second pixel from top is read out.

multiple chips connect to a single sensor, operating only one chip can cause voltages on neighboring chips to rise to unsafe levels. Therefore, all wirebond pads for chips not being tested are kept at the common ground. During IV testing, all chips are grounded. To facilitate this, a grounding plate was designed and built at the University of Tennessee workshop and added to the probe station's chuck. This grounding plate features metal flaps that can be precisely positioned over the wirebond pads using a screw (see close-up view in Fig. 1). A 100 μm thick and 5 mm wide conductive nylon fabric tape is conductively glued to the underside of each flap, providing both mechanical flexibility and reliable electrical contact across all wirebond pads. Pre-bending the flaps guarantees enough spring force with even and firm pressure against the pads. The plate and chuck serve as heat sinks, supported by an air fan. Two complementary charge-injection methods have been developed to characterize open bumps. The CROC operational parameters are tuned to a threshold of 2000 e^-. The efficiency of each pixel is scanned as a function of the injected signal amplitude. For well-tuned pixels, this function has a characteristic sigmoid shape (S-curve). The inflection point corresponds to the pixel's threshold, while the slope is related to its noise [15]. In the **Threshold–Noise Method**, S-curves are taken under reverse bias (-80 V) and slight forward bias (+1 V). The noise depends on the sensor's capacitance, which varies with the depletion depth. Forward bias reduces this depth and induces a current of opposite sign compared to the charge signal, thereby decreasing it at the input node of the analog front-end. As a result, additional charge must be injected to achieve the same net signal. Pixels that are not properly connected show little to no change in either parameter. Pixels with both shift values below a set threshold are marked as disconnected (see Fig. 3). In the **Crosstalk Method**, a large signal ($39,000$ e^-) is

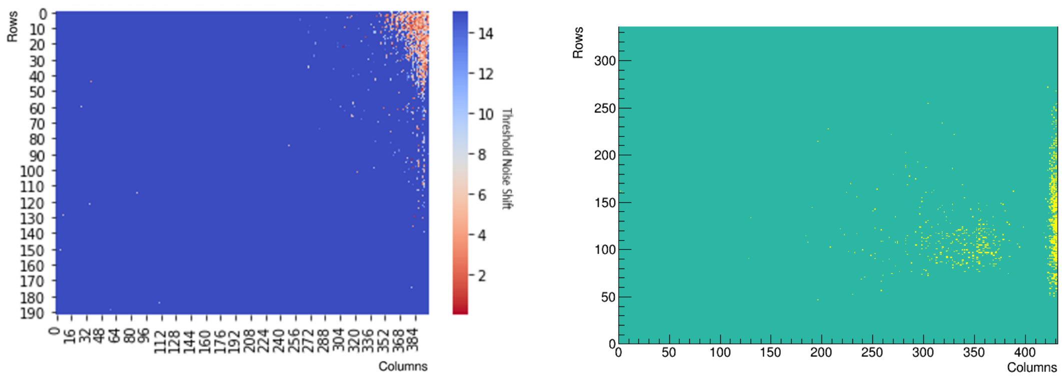

Figure 3: CROC pixel rows versus columns. Left: Problematic pixels identified through minimal shift in noise and threshold for different bias voltages are shown with color coding. Right: Disconnected pixels identified via the crosstalk method are highlighted in yellow.

injected into a specific pixel, and the response of neighboring pixels due to capacitive coupling is measured. Silicon sensors with rectangular pixels of pitch $25 \times 100\ \mu\mathrm{m}^2$ do not match the CROC's bump pad pitch of $50 \times 50\ \mu\mathrm{m}^2$. This layout causes varying spatial relationships between injected and neighboring pixels, resulting in two different levels of capacitive coupling (see Fig. 2). The coupled case shows stronger crosstalk in nearby pixels due to geometric proximity and increased capacitive coupling, while the uncoupled case results in more isolated signal responses. Using both injection patterns helps reduce misclassifications caused by defective neighboring pixels. Pixels with responses below 10% for both patterns are flagged as missing, those above 95% are considered functional, and the remaining are labeled as problematic. The reliability of injection methods was confirmed using X-ray and radioactive source measurements, which are more complex to set up and slower.

4. Results

Over 200 CROCs bump-bonded to sensors, mainly of the 2×1 type, have been tested. This includes nine iterations with one vendor to gather feedback for refining the bump-bonding process. Several issues in sensors and chips have been identified. Fig. 4 (left) shows three examples of IV curves, consistently measured at 20^o C with light shielding. Typically, the current plateaus at a reverse-bias voltage above 10 V. For a series of modules, ohmic behavior was observed at bias voltages above 60 V (dotted curve). Very few exhibited an immediate rise in current (dashed line). Fig. 4 (right) shows the number of open bump-bonds per CROC for less than 10 and more than 10, respectively. Early sets of bare modules are located on the right side. Chips with 600 or more open bumps are rejected. CROCs with clusters of 50 or more open bumps are also rejected.

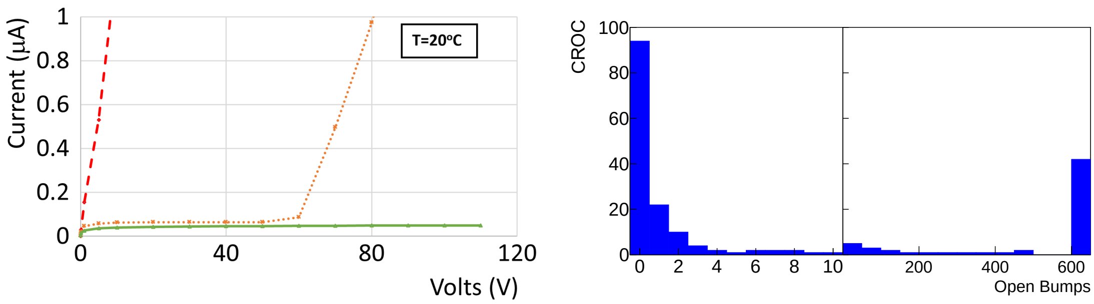

Figure 4: Left: IV curves showing regular (green solid), ohmic (orange dotted), and breakthrough (red dashed) behavior. Right: Open bump-bonds per CROC as detected by the cross-talk method. Note that all entries greater than 600 are in the last overflow bin.

5. Summary

Quality control on the bare modules has become a key part of the CMS inner tracker module pre-production process, ensuring early-stage quality inspections during assembly. The bump bonding process has been improved and validated with vendors. To date, over 200 readout chips have been tested. Testing is expected to be applied on a sampling basis during full production and will remain a valuable diagnostic tool throughout the project's lifetime.

Acknowledgments

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