

Time-resolved Studies of Single-Event-Upset Effects in the Optical Data Receiver for the First LHC Upgrade Phase of the ATLAS Pixel Detector

M. Ziolkowski¹

Universität Siegen

Department für Physik, D-57068 Siegen, Germany

E-mail: michael.ziolkowski@uni-siegen.de

P. Buchholz

Universität Siegen

Department für Physik, D-57068 Siegen, Germany

E-mail: buchholz@hep.physik.uni-siegen.de

A. Wiese

Universität Siegen

Department für Physik, D-57068 Siegen, Germany

E-mail: andreas.wiese@uni-siegen.de

K. K. Gan

The Ohio State University

Department of Physics, 191 West Woodruff Ave., Columbus, OH 43210, USA

E-mail: gan@mps.ohio-state.edu

H. Kagan

The Ohio State University

Department of Physics, 191 West Woodruff Ave., Columbus, OH 43210, USA

E-mail: kagan@mps.ohio-state.edu

R. Kass

The Ohio State University

Department of Physics, 191 West Woodruff Ave., Columbus, OH 43210, USA

E-mail: kass@mps.ohio-state.edu

S. Smith

The Ohio State University

Department of Physics, 191 West Woodruff Ave., Columbus, OH 43210, USA

E-mail: ssmith@mps.ohio-state.edu

¹ Speaker

An optical receiver board housing an amplifier-and-decoding ASIC designed in 130 nm CMOS process for use with bi-phase-mark encoded input signals, coupled to a PiN-photodiode array, was exposed to a proton beam of 24 GeV/c momentum at CERN. At the same time a reference receiver board containing the same ASIC but coupled to an electrical input-signal-source was also exposed to the proton beam. The 40 MHz clock and 40 Mbps data signals encoded together and supplied to the devices under test, were restored directly on both boards and then transmitted back to the counting room for on-line checking of consistency. In the case of a data-bit error or a missing clock transition, indicating an occurrence of a SEU, a sequence of time aligned data-bits and corresponding clock-states were recorded and in part as oscilloscope-waveforms for off-line analyses. Measurements were performed using a custom-developed FPGA-based DAQ system, for input signals covering a certain range of optical and electrical amplitudes. We present results obtained from the 2010 run at the CERN irradiation facility, including the SEU rate and cross-section dependence on input signal amplitude, for various types of effects on clock and data consistency, along with the time-resolved structure of the SEU incidents.

10th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors
Firenze, Italy
July 6-8, 2011

1. Introduction

The Large Hadron Collider (LHC) at CERN will be upgraded in two phases to increase its luminosity. During the first upgrade phase in 2013-2014 a new layer of pixel detector (inner b-layer, IBL) will be added to the existing tracking system of the ATLAS experiment. The larger amount of data expected from the IBL will be handled by an upgraded optical link. The on-detector part of the optical link will be built as a new generation of multi-channel opto-electrical transceiver assemblies (opto-boards). In the receiver part of the opto-board, a PiN-photodiode array is connected to a custom developed receiver and decoding ASIC (DORIC) for signal amplification and for subsequent recovery of the 40 MHz clock signal along with the decoding of a 40 Mbps data stream (timing-trigger-and-control signal, TTC), which are transmitted optically to the opto-board as bi-phase-mark (BPM) encoded signal. The newly developed DORIC chip is a prototype in 130 nm CMOS technology [1]. It consists of three transmission channels and one spare channel. In parallel to irradiation tests addressing opto-board performance as a function of accumulated irradiation dosage, the optical receiver part of the opto-board was studied in August 2010, regarding instantaneous effects of Single-Event-Upset (SEU) on the integrity of the clock and data output signals. The study we report has been performed in a similar way to our previous SEU test conducted one year earlier [2] on an assembly consisting of the first generation DORIC chip in 0.25 μm CMOS technology [3], connected to a fast PiN-photodiode array [4] and subjected to newly developed approach of time-resolved SEU analyses. A similar time-resolved error-logging approach was adopted earlier for a set of comprehensive SEU studies at Multi-Gbps data transmission rates [5]. In [2] we have discussed the SEU rate prediction in the ATLAS pixel detector, resulting in one bit-error in 20 minutes per transmission channel and reaching one bit-error in 80 seconds at the end of the detector life time. It is well known from earlier radiation-induced SEU studies [6]-[8], that the optical PiN-photodiode receiver itself is the device most vulnerable to the instantaneous impact of radiation on transmitted signals due to its comparatively large SEU sensitive area. The PiN-photodiode coupled trans-impedance-amplifier (TIA) is also reported to contribute to the occurrence of SEUs. It is the relatively low-current input-signals that make the TIA-components sensitive to SEU incidents. In the optical receiver of our application, the final pattern of SEU induced errors emerges from the BPM-decoding part of the DORIC chip, where the input signal, in particularly the one distorted by SEU incident in the PiN-photodiode or in the TIA-part, is continuously processed by the logic of clock and data recovery. The goals of our present SEU studies include the prediction and measurement of the SEU occurrences, to learn about occurring error patterns and to increase the understanding of possible mitigation strategies.

2. Experimental setup for time-resolved Single-Event-Upset measurements

The optical receiver used for this study consists of a commercially available 4.25 Gbps GaAs PiN-photodiode array [9] connected to our latest 4-channel DORIC chip. The optical receiver is a prototype for the future ATLAS pixel IBL project. The block-diagram of the experimental setup is shown in Figure 1. On the FPGA board a pseudo-random 40 Mbps data-bit-stream is

continuously generated, BPM-encoded with a 40 MHz clock and optically transmitted over 20 m for subsequent decoding to the optical receiver exposed to the proton beam. Both recovered LVDS signals, data and clock, are transmitted electrically back to the FPGA board for checking of their consistency. Four receiver assemblies are tested simultaneously. Two of them are supplied with a regular optical BPM input signal of adjustable optical amplitude. The other two, which do not contain a PiN-photodiode array, are supplied instead electrically with current input signals of selected amplitudes. The returned data-bits are sampled by a 40 MHz reference clock on the FPGA board and compared to the data-bits originally generated. A difference in the compared bits causes the next 4 clock cycles to be recorded, as well as the preceding 4 cycles. As with the data-bits, the alternating states of the returned clock are continuously sampled by an 80 MHz reference clock. This allows us to keep track of the clock's transition from 1 to 0 and back to 1. Both clock-state sequences 1-0-0 and 0-1-1 are considered to be clock errors and are also used by the test-system to trigger the event recording. For each event recorded, its time of occurrence, with a resolution of 25 ns, is saved as well. The test-system can store up to 2700 events in a buffer before being read out by the DAQ computer.

3. Single-Event-Upset measurement run

The time-resolved SEU measurement was performed at CERN's proton irradiation facility [10] in August 2010. The use of 24 GeV/c protons for studying the SEU effects in the ATLAS inner-detector's opto-electronics is justified by similar magnitude of the SEU formation relevant non-ionizing cross-sections of 300 MeV/c pions, which dominate the particle flux in the ATLAS detector, and those of 24 GeV/c protons, both in Si and in GaAs [11]. The SEU data was taken independently on four optical channels of a PiN-photodiode array connected to a DORIC receiver chip. The optical power of the input signal was attenuated to six values between 100 and 600 μA and controlled by measuring the photocurrent amplitude in the PiN-photodiode. The PiN-photodiode was reversed-biased at +10 V. The lowest optical power of 100 μA , just about four times the DORIC threshold input current, is equivalent to the lowest expected PiN photocurrent [12]. The highest optical power setting of 600 μA corresponds to the twice expected average PiN photocurrent of 300 μA at detector's location, where the opto boards are going to be installed [12]. For the additional two test assemblies without the PiN-photodiode, the input current amplitude was fixed electrically at three values of 100, 200 and 400 μA ; each one was assigned to two DORIC channels. For each optical power input setting the beam exposure time was on average 250 proton-bursts, each 430 ms long, with a 40 s beam-cycle period, each comprising two bursts. This corresponds to an average exposure time of nearly 108 s at each optical power setting, or 4.4 billion of data-bits transmitted. The average proton flux of $3.5 \times 10^{11} \text{ cm}^{-2} \text{ s}^{-1}$ during the SEU test was deduced from the total proton fluence measured with the Al-strip activation method [10]. In between the proton-bursts the data monitoring was active in order to provide a SEU-free reference measurement.

4. Classification of Single-Event-Upset incidents

Similar to the SEU analyses of 2009 run, three categories of upset-incidents are considered in the 2010 run as well:

- **Type-D** (Data) with only data-bit errors observed but no clock deficiency,
- **Type-C** (Clock) with clock deficiency but no data-bit errors,
- **Type-B** (Both) with both data-bit errors and clock deficiency.

A total of **82412** events were collected in this study for channels with PiN-photodiode connected to the receiver chip. Among them are **65052** events of type-D, **8840** events of type-C and **8620** events of type-B. The frequency of SEU occurrence for typical conditions of transmitted data-bits and recovered clock-states is summarized in Table 1. The underlying selection was done by considering the number of bit-flips as well as affected clock-states per SEU incident and in parallel by distinguishing between two types of clock-state deficiencies (H→L, L→H swaps) and two bit-flip modes (0→1 and 1→0). As a result of this classification there are 10 SEU classes listed in Table 1. Only 29 additional bit and clock errors were detected in between the bursts, when the proton beam was off and the recovered signals were monitored. As a result of this analysis an intrinsic bit-error rate of 0.8×10^{-11} was estimated.

5. Single-Event-Upset rate and cross-section

The experimentally obtained SEU rate, calculated as a ratio of the SEU occurrence and the amount of data-bits transmitted during 400 ms of spill duration, is shown in Figure 2 as a function of the input signal amplitude as given by the photocurrent in the PiN-photodiode. The observed SEU rate decreases by a factor 3 in response to the increase of input photocurrent from 100 to 400 μA . In comparison, nearly the same factor of 3 was measured earlier for input photocurrent raise from 50 to 100 μA [2]. Hence, the effectiveness of SEU rate mitigation by boosting light signal amplitude becomes limited with increasing input photocurrent. It is evident from the decomposition of the total SEU rate into D, C and B contributions (Table 1, Figure 2), that the type-D events clearly dominate the SEU rate for all optical power settings with 79% probability of occurrence, whereas for type-C and -B events a relative contribution of nearly 10% each was observed. This is almost the same result we obtained from 2009 measurement [2], which was limited by 110 μA maximum input photocurrent. The newly measured SEU cross-section is presented in Figure 3. It is defined as a ratio of the SEU occurrence (per unit of time) and the corresponding proton flux, given as a function of the input signal photocurrent. The underlying data includes contributions from all event types and results from averaging four PiN-channels, for which the measurements were simultaneously performed. The cross-section's relative error of 18% arises from channel averaging (16%) and from the uncertainty in the determination of the total proton fluence (8%) [10]. A scaling factor of 8, derived in section 6.5, has been applied. A comparison with our earlier SEU cross-section measurements reveals good agreement at 300 μA [3], at 100 μA [2] the present result is lower by a factor 3 and at 500 μA [3] higher by a factor 5.

6. Time-resolved results

6.1 Type-D events

Type-D events (cases 1 ÷ 3 of Table 1) dominate the total SEU rate with a probability of nearly 80%. Their signature is simple: a single data-bit error for each SEU incident, with 0-to-1 bit-flip

upset occurring most of the time (97%) and 0-to-1 transition suppressed down to level of 3%. Hence for PiN-photocurrents exceeding 100 μA only the 0-to-1 error-mode is of practical concern. Type-D events with two data-bits flipped (case 3) are very rare ($\sim 0.1\%$). Creation mechanism of type-D events is well understood and was discussed in detail in [2]. The SEU rate dependence on the photocurrent amplitude is shown in Figure 4. In the given region of high input photocurrent amplitude a further powerful mitigation of type-D events can be achieved by use of forward-error-correction (FEC) method. The FEC can be implemented by data-bit stream encoding with e.g. one of the Hamming codes. This has been demonstrated [5] for non-BPM data transmission specifically.

6.2 Type-B events

The measured relative rate of type-B events, with both data and clock errors, is about 10%. Depending on the type of the clock deficiency, these events can be split up in two classes. The first class consists of events characterized by inverted-clock-cycles and relative occurrence of $\frac{3}{4}$; cases 6 \div 8, Table 1. To the second class belong events with interrupted-clock and $\frac{1}{4}$ of relative occurrence; cases 9 \div 10. All identified patterns of corrupted clock signal are provided in Table 1. Dependence of the SEU rate on the photocurrent amplitude is given in Figure 5.

- Inverted-clock events are correlated with a high number of data-bits set to ‘1’ transmitted in a single-chain, as already discussed in [2]. The majority of inverted clock events show only one clock cycle with both high and low states reversed; case 6. About $\frac{2}{3}$ of them are associated with 0-to-1 and $\frac{1}{3}$ with 1-to-0 bit error transition. Events with higher number of affected clock cycles, up to 4, amount all together to 42% of inverted-clock events and are accompanied by two data-bit errors, one at the beginning and one at the end of the sequence respectively. The first bit error is of type 0-to-1, whereas the second one favors 1-to-0 transition.
- Interrupted-clock events are characterized by missing high state of the clock. This happens almost exclusively for only one clock cycle; case 9. On rare occasions ($\sim 2\%$) up to 4 consecutive clock states are affected; case 10. This class events are accompanied by mostly one and seldom ($\sim 6\%$) two data-bit errors, with favored 1-to-0 transition.

In Figure 6 we show examples of recovered clock signal for type-B events, recorded on-line as waveforms by oscilloscope. In particular, clock signal discontinuity lasting a few cycles long may conditionally upset a subsequent clock consumer. Possible mitigation strategy for type-B events is feasible on circuit design level only. Type-B events result namely from interplay of BPM-encoded input signal, distorted by SEU incident in the PiN-photodiode directly or inside the TIA-part, and the circuit logic of clock-recovery and data-decoding implemented in the receiver chip. The clock recovery of the DORIC circuit depends strongly on the presence and quality of each clock leading edge transmitted; in the course of this, trailing edges of recovered clock are always derived from the leading edges. Regarding the SEU immunity of the clock-recovery and subsequent data-decoding, better results could be expected from a PLL (phase-locked-loop) based clock-recovery mechanism, instead of a pure DLL (delay-locked-loop) based one, as implemented on the DORIC chip. Given that the measured rate of complex type-B events is clearly lower than the contribution from simple type-D events, no mandatory

mitigation of them is required. For other applications, with even higher demand on recovered clock integrity, a PLL circuit solution might be a better choice.

6.3 Type-C events

Type-C events, characterized by only one high clock-state missing and no data-bit errors, were measured with a relative rate close to the rate of type-B events (~10%). Alternatively one can regard type-C events as incidents belonging to the interrupted-clock class (analogous to case 9, Table 1) but with no affiliated data-bit errors. For less than 2% of type-C events more than one clock cycle becomes changed. These latest events are analogous to the inverted-clock class, with no data-bit errors associated. From the clock consumer point of view, it is important to stress, that for all SEU events of type-B and -C, the recovered clock signal always returns to its original phase.

6.4 Fraction of SEU incidents on receiver chip only

Six DORIC channels not connected to the PiN-photodiode, were supplied with an input current signal generated electrically. Three signal amplitudes of 100, 200 and 400 μA were selected. Each one was applied on two channels and kept constant during the whole run. The electrical channels contributed in total to **3070** SEU events, with **2264** of type-D, **268** of type-C and **538** of type-B. Corresponding error patterns were found to be very similar to those seen on optical channels, with a dominance of type-D events and secondary importance of type-C and -B events. The rate of type-D events here turns out to be slightly lower (74% instead of 79%) but the rate of type-B events is slightly higher (17% instead of 10%), while the contribution of type-C events remains nearly unchanged. In Figure 7 the corresponding SEU rate dependence on the input current amplitude is shown. By comparing the SEU rates on channels tested with and without PiN-photodiode, we conclude that the SEU incidents occurring on the receiver chip only amount to less than 4% of the total rate measured for the whole optical receiver.

6.5 Time distribution of SEU event during the spill

The occurrence time of each SEU incident is known in our measurement with a resolution of 25 ns. In Figure 8 two distributions of event occurrence time are shown: for PiN-photodiode channels connected to the receiver chip and separately for receiver channels without PiN-photodiode connected but with an electrically applied input current signal. The proton flux during each spill is typically ramped up within ~50 ms at the beginning of the spill and stays nearly constant at its high plateau level until the end of the spill ~370 ms later, then it vanishes rapid in less than 10 ms. In our measurement, the SEU events detected on channels with the PiN-photodiode connected to the receiver chip, occurred predominantly in a time window of ~50 ms (width at half maximum) at the beginning of the spill. At later times in the spill window the distribution of events becomes low and nearly flat. In contrast, events which originated from SEU incidents on the electrically supplied receiver chip occurred in a wider range of the spill window, as one would expect to happen in both cases. We assume that the above result is caused by the ultra high proton flux of $3.5 \times 10^{11} \text{ cm}^{-2} \text{ s}^{-1}$ that the PiN-photodiode is exposed to. The 25 GeV/c proton beam line is optimized for irradiation studies aiming to accumulate a large

radiation dosage within a short time. At the beginning of each spill, when the proton rate is ramped up, the SEU events are induced as expected, by creation of charge in the PiN-photodiode volume through secondary ionization. The maximum SEU rate is reached close to the time of the proton flux saturation, and then it becomes depleted and stays suppressed until the end of spill. In this manner, the SEU events seen after the distribution-peak are most likely caused by SEU events created on the receiver chip itself. These observations are preliminary and will be investigated further. For the purpose of the SEU cross section determination a correction scaling factor of 8 has been estimated by comparing the total number of events contributing to the distribution-peak with the product of the distribution maximum value and the spill duration. In order to provide a conservative upper limit on the SEU cross section, the data shown in Figure 3 has been accordingly scaled.

7. Summary

We have analyzed SEU data obtained in 2010 for an optical receiver assembly built as a prototype for the IBL upgrade of the ATLAS pixel detector. The SEU data was collected using an approach of time-resolved measurement, similar to our first measurement of this type one year earlier. The rates for various error conditions of reconstructed data and clock signals were obtained and analyzed for a range of input signal current amplitudes between 100 and 600 μA . We have performed measurements on two assemblies in parallel, with and without a PiN-photodiode connected to the custom developed receiver ASIC, in order to distinguish between SEU occurrences in the PiN-photodiode and on the receiver chip. Our findings are summarized below.

- The main SEU contribution, almost 80% of all cases, has the simplest possible error structure of exactly one data-bit flip of mostly 0-to-1 transition. The fraction of 1-to-0 data-bit transition is on the level of few percent. Effective mitigation of these events is possible by employing a FEC-scheme at the expense of extended length of transmitted data-bits. This would be an option to be considered in case the SEU rate becomes unacceptable.
- Approximately 20% of all SEU events show the decoded clock signal being affected as well. Half of that amount is identified as events with only one high clock-state missing and no data-bit errors. The second half is populated by events with both clock-state and data-bit errors, subdivided into two error classes: inverted-clock with high and low states interchanged and interrupted-clock with the high state missing. Inverted-clock events were found to occur three times more frequently than interrupted-clock events. Both error classes occur mostly with exactly one clock cycle affected. Bursts with a few clock cycles upset were observed as well, but less frequently. Events of both classes are accompanied by one and not more than two data-bit errors.
- Events with clock deficiency originate from a combined interaction of SEU occurrence in the PiN-photodiode or in the TIA-part of the receiver chip and the recovery and decoding scheme implemented on the receiver chip. SEU mitigation here would be feasible only by adopting another clock recovery scheme; e.g. a PLL based one. This was not required for the current optical receiver, which was designed a-priori for use with BPM encoded input signal only.

- A fraction of SEU events occurring exclusively on the receiver chip, most probably in the TIA-part, has been obtained by using a few receiver chip channels not connected to the PiN-photodiode but supplied electrically instead. The on-chip occurring events reveal a similar pattern of data-bit and clock-state errors and are characterized by the nearly same relative occurrence rates, as those of the PiN-photodiode connected to the receiver chip. The measured fraction of the SEU on-chip occurrences amounts in total to less than 4% of all events.
- By analyzing the time distribution of the SEU occurrences with respect to the proton spill time profile, it was observed, that the SEU counting rate for the PiN-photodiode connected to the receiver chip grew steadily at the beginning of each proton spill and declined onward to the level of on-chip occurrences after the proton flux reaches its high intensity plateau. We will follow-up this observation with more studies in the future.

Acknowledgements

The authors would like to thank Maurice Glaser from the CERN irradiation facility for his great help and assistance during the 2010 run. This work was supported in part by the U.S. Department of Energy under contract No. DE-FG-02-91ER-40690 and by the German Federal Minister for Research and Technology (BMBF) under contract No. 05H09PSA.

References

- [1] K.K. Gan et al, *Radiation-hard ASICs for Optical Data Transmission*, contribution to RD11 conference.
- [2] M. Ziolkowski et al, *Time Resolved Studies of Single Event Upset in Optical Data Receiver for the ATLAS Pixel Detector*, contribution to RD09 conference.
- [3] K. E. Arms et al, *ATLAS pixel opto-electronics*, Nucl. Instrum. Methods, A **554**, 458-468 (2005).
- [4] Optowell Co., Ltd., AP85-2M112 2.5/3.125 Gbps GaAs 1x12 PIN-PD Array, data sheet rev. 1.1.
- [5] A.J. Pacheco et al, *Single-Event Upsets in Photoreceivers for Multi-Gb/s Data Transmission*, IEEE Transactions on Nuclear Science, Vol. 56, No. 4, 1978-1986 (2009)
- [6] P. Marshall et al, *Space Radiation Effects in High Performance Fiber Optic Data Links for Satellite Data Management*, IEEE Trans. on Nucl. Sci., Vol. **43**, No. 2, 645-653, (1996).
- [7] F. Faccio et al, *Single Event Upset Tests of an 80-Mb/s Optical Receiver*, Nucl. Instrum. Methods, Vol. **48**, No. 5, 1700-1707 (2001).
- [8] J.D. Dowell et al, *Single event upset studies with the optical links of the ATLAS semiconductor tracker*, Nucl. Instrum. Methods, A **481**, 575-584 (2002).
- [9] U-L-M PHOTONICS, *4 Gbps PIN Photodiode Chip*, data sheet PIN-ULM-04-TN_V6.
- [10] M. Glaser, <https://irradiation.web.cern.ch/irradiation/>
- [11] A. Chilingarov et al, *Radiation-Induced Damage in GaAs Particle Detectors*, IEEE Trans. on Nucl. Sci., Vol. **44**, No. 5, 1705-1707 (1997) (and references inside).
- [12] T. Flick, *Optical fibers, cables, connectors*, FDR Optical Link presentation, <http://www.atlas.uni-wuppertal.de/optolink/FDR/>, 26 (2003).

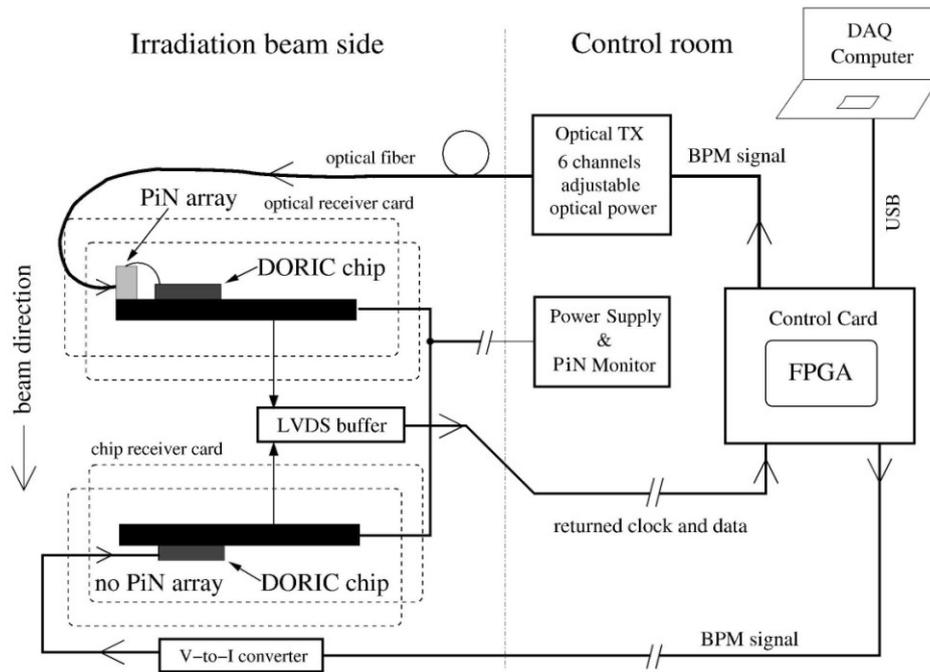


Figure 1:

Block diagram of the experimental setup used for the time-resolved SEU measurement during the 2010 run.

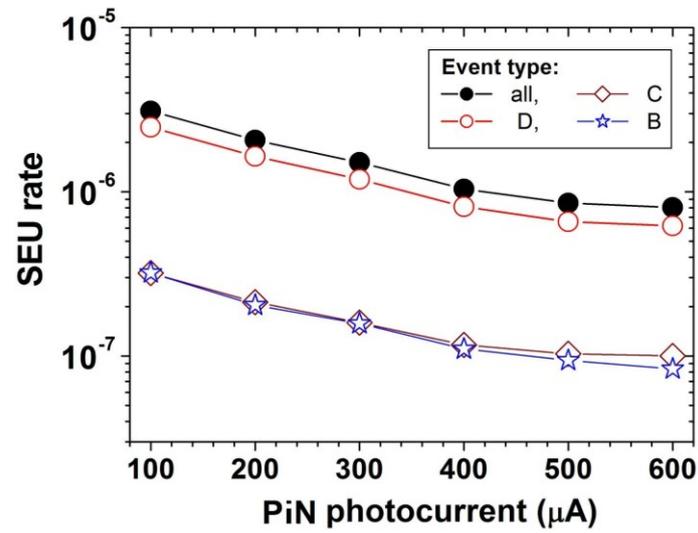
Type D ~79% only data affected 16263 events	# Bit-flips		Bit-flip type	Case
	one 100%	0→1 97%		1.
		1→0 3%		2.
two ~0.1%	both		3.	

Type C ~11% only clock affected 2210 events	# Clock states		Clock deficiency	Case
	one 98.3%	H→L 100%		4.
	≥ two 1.7%	inverted		5.

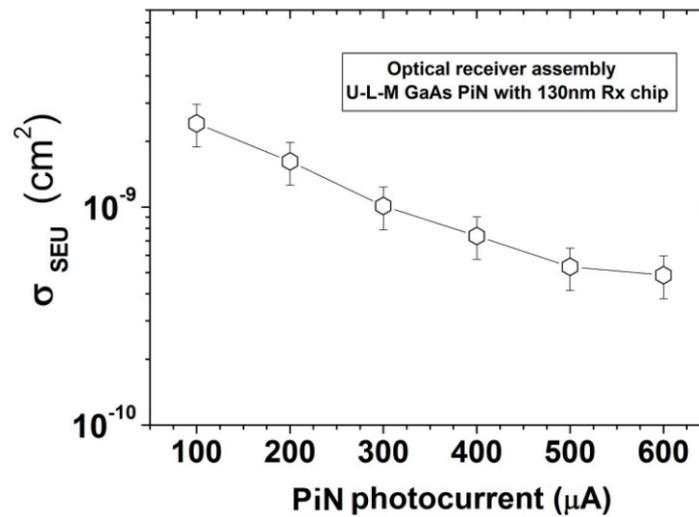
Type B ~10% both clock and data are affected 2130 events	Clock deficiency type			# Bit-flips	Bit-flip type	Case
	inverted 1625 ~ 76%	933	1 0 (0 1) _n 1 0 1 with n = 1			
		557	1 0 (0 1) _n 1 0 1 with n = 2, 3, 4	two	$\left\{ \begin{array}{l} 1^{\text{st}} \text{ bit:} \\ 0 \rightarrow 1 \text{ 98\%} \\ 1 \rightarrow 0 \text{ 2\%} \\ 2^{\text{nd}} \text{ bit:} \\ 0 \rightarrow 1 \text{ 38\%} \\ 1 \rightarrow 0 \text{ 62\%} \end{array} \right.$	7.
						135
	interrupted 505 ~ 24%	494	1 0 (0 0) _n 1 0 1 with n = 1	one 94%	$\left\{ \begin{array}{l} 0 \rightarrow 1 \text{ 33\%} \\ 1 \rightarrow 0 \text{ 67\%} \end{array} \right.$	9.
11		1 0 (0 0) _n 1 0 1 with n = 2, 3, 4	two 6%	10.		

Table 1:

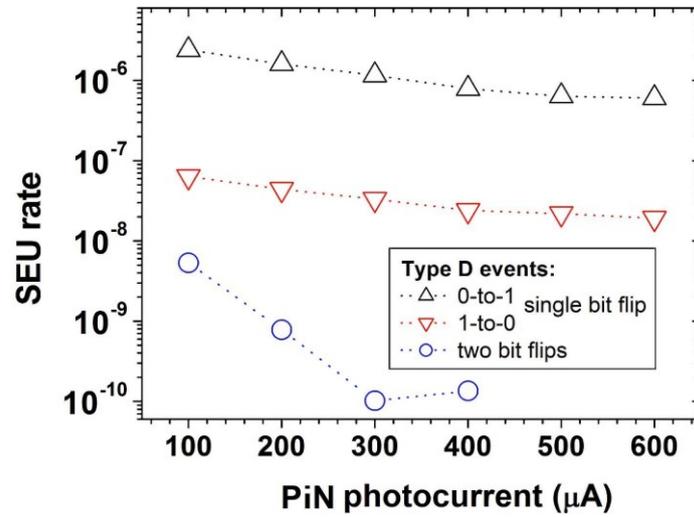
SEU frequency of occurrence for various conditions of recovered clock and transmitted data compiled for events of type-D, -C and -B. The event rates are given per a single optical receiver channel.

**Figure 2:**

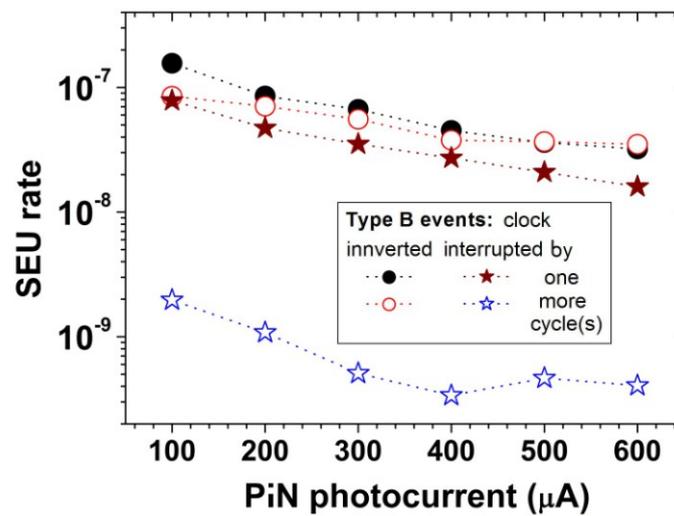
Dependence of the SEU rate as a function of the PiN photocurrent for all event types.

**Figure 3:**

Measured SEU cross-section as a function of the PiN photocurrent.

**Figure 4:**

Dependence of the SEU rate for type-D events, case resolved, as a function of the PiN photocurrent.

**Figure 5:**

Dependence of the SEU rate for type-B events, case resolved, as a function of the PiN photocurrent.

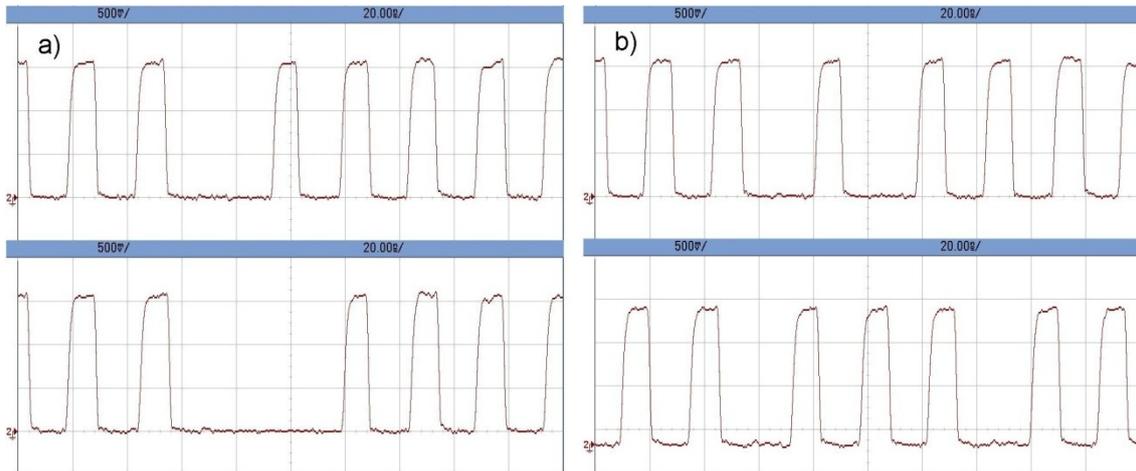


Figure 6:

Output clock signal for type-B events recorded on-line on an oscilloscope:
 a) interrupted-clock (case 9 ÷ 10, Table 1) with one and two cycles affected,
 b) inverted-clock (case 8, Table 1) with basically one and three cycles affected.

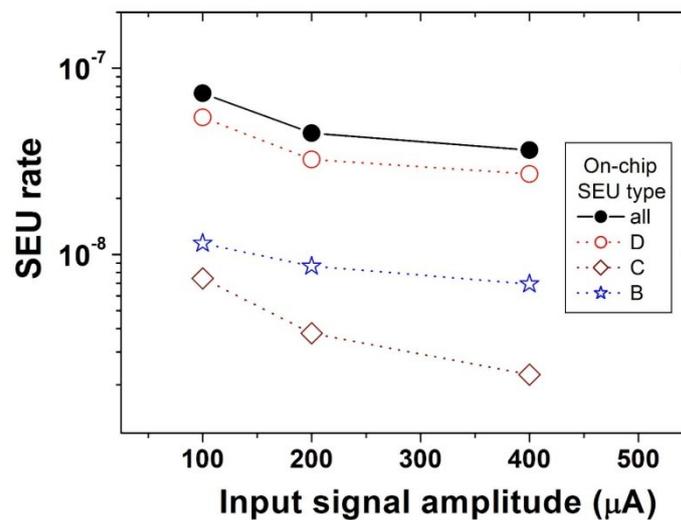


Figure 7:

Dependence of the SEU rate occurring on the receiver chip only, type resolved, as a function of the input current amplitude.

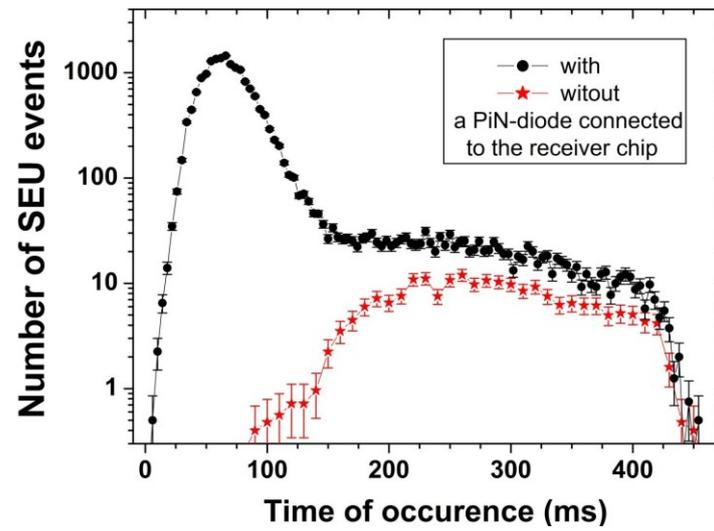


Figure 8:

SEU time of occurrence distribution inside the proton-spill time window, with and without a PiN-photo-diode connected to the receiver chip.