PROCEEDINGS OF SCIENCE

State of the art in Microfabrication

Jurriaan Schmitz[1]
MESA+ Institute for Nanotechnology, University of Twente
P.O. Box 217, 7500 AE Enschede, Netherlands
E-mail: J.Schmitz@utwente.nl

In this review paper the state of the art in microfabrication is presented. The focus is on trends in integrated circuit fabrication by mainstream industrial players. The article starts with Moore's Law, describing its inception as well as the evolution of Moore's metric of the number of components per chip until today. Then, the main trends in manufacturing and in contemporary research are sketched, for CMOS integrated circuits, memory chips, and other planar technologies. The field is rapidly expanding beyond silicon for future microelectronic devices, fired by market demands in various fields such as LED lighting, photovoltaic systems and power electronics. Emerging semiconductor materials are reviewed in the perspective of radiation detection potential in the final section.

Technology and Instrumentation in Particle Physics 2014
2-6 June, 2014
Amsterdam, the Netherlands

[1] Keynote Speaker

PoS(TIPP2014)017

1. Moore's Law

Microfabrication took off in the 1960s after researchers at Fairchild proposed planar technology for semiconductor devices in 1958 [1]. The idea of planar technology is simple but powerful: starting with a well-chosen (bulk) substrate material, patterns are formed *on a single side* by a sequence of fabrication steps. Processing on one side of the material is somewhat restricting the possible device architectures and configurations, but it has enormous practical advantages, in particular for electrical interconnection.

Integrated circuits soon followed the proposal of planar technology for semiconductor devices. The first were produced by Jack Kilby at Texas Instruments (Nobel Prize 2000 [2]) and by Jean Hoerni and Robert Noyce at Fairchild [1]. With their work they showed that one fabrication approach, on one starting material, could provide the basic electrical components (transistors, resistors, capacitors and inductors) necessary to make complete electronic circuits.

At first, a considerable part of the community was reluctant to adopt this new approach. Some people argued that production yields of integrated circuits could never reach an acceptable level, which turned out incorrect [2]. More fundamental was the objection that the fabrication of all components from the same material inherently led to a suboptimal choice of materials, not leading to the best possible device specifications. After all, good resistors were made of a different material than transistors, or inductors. To make all devices by planar technology, and from the same material, even today is counterintuitive to a community that strives to make electronics with the best possible performance.

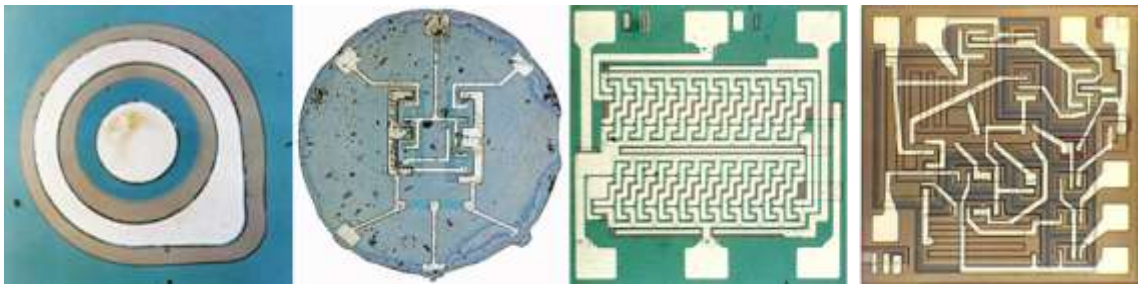

Figure 1: Rapid progress of commercially produced integrated circuits in the period 1958-1965. From left to right: the first planar transistor (Fairchild 1958), the first integrated circuit with planar interconnect (Fairchild 1961), the first MOS circuit (GMe, 1964), and the first widely used analog IC (µA709, Fairchild 1965). Images courtesy of the Computer History Museum [3].

Events that followed, disproved these arguments in the 1960s, as the integration complexity of mass-manufactured semiconductor circuits rapidly rose (Figure 1). Gordon Moore captured this trend in his famous 1965 article in Electronics [4]. Moore recognized that transistors (or generally: components) became progressively cheaper to manufacture by the piece, using this newly developed planar technology. He identified three main underlying causes of this decreasing price: (1) components were miniaturized; (2) chips and wafers got (slightly) larger over time; and (3) better manufacturing skills were developed. As a result of

this declining component price, there was an economic rationale to produce and sell chips with more and more components on board. Moore observed that until 1965, the number of components on a chip had been doubling every year; and he saw no reason why this trend would not continue through 1975.

In 1975, Moore commented on his prediction at the International Electron Device Meeting [5]. While new data still supported his original claims, he predicted that a slowdown of the complexity increase to a factor 2 per two years (rather than 1 year) would occur around 1980. Basically he expected that the third underlying cause mentioned above would run out of steam around that time. The industry has indeed roughly followed this trend in the last few decades, as can be seen in Figure 2 – be it that the kink appeared earlier in time.

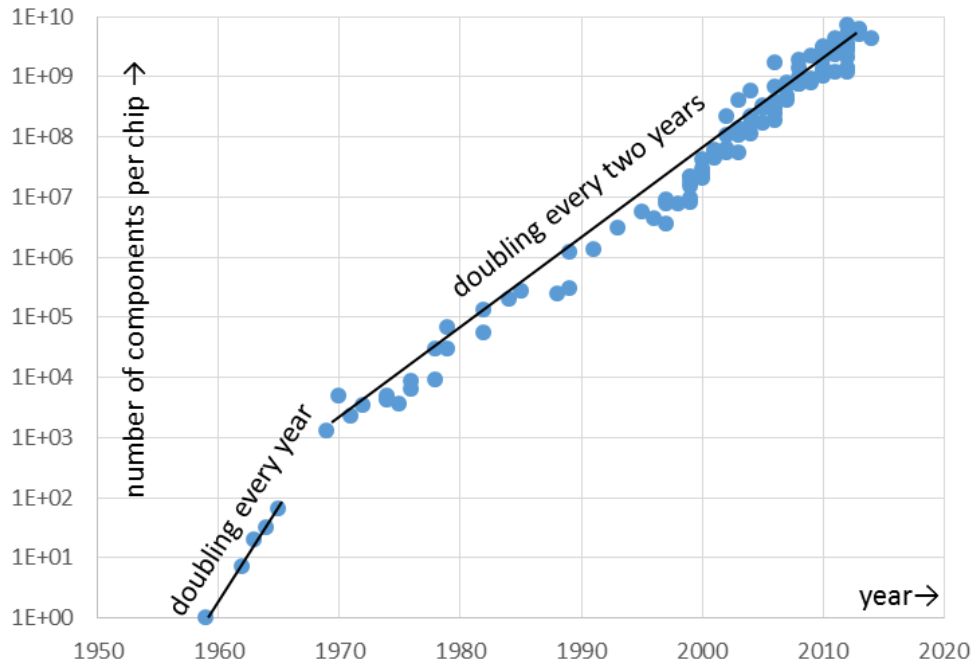

Figure 2: the number of components on a chip over the years. The first five data points are from Moore's original article [4]. Later data, only including CPUs and GPUs, are provided by over 30 IC manufacturers and summarized in [5,6]. The lines are drawn to guide the eye.

Looking at microprocessors alone, this trend is no longer followed in recent years. After the CPU (central processing unit) clock frequency has stabilized[2] around 3.4 GHz in 2005, multicore processors were introduced, and the increase in transistor count of CPUs slowed down. In the last decade, graphical processor units (GPU's) have consistently beaten CPU's both in transistor count and in the number of floating point operations per second (FLOPS). Field-programmable gate arrays (FPGA's) and memory chips have even higher transistor counts than the CPU's and GPU's in Figure 2.

[2]This stabilization is related to the power dissipation in the circuit (linearly proportional to the clock frequency) and the difficulty to maintain the silicon die at a reasonable operating temperature.

Since 1994, a consortium of the semiconductor industry has periodically published a roadmap, the International Technology Roadmap for Semiconductors (ITRS). The most recent roadmap [7] forecasts new CMOS generations to emerge every 3 years in the coming decade, rather than every 2 years. For DRAM memories, scaling is extremely complex and doubling of the number of bits per chip every 4 years is projected. Only the number of bits in Flash memories is still expected to double every 2 years in the coming decade – be it not by a rapid increase of the number of components through miniaturization, but rather through multi-level storage and vertical stacking of bits, so-called 3D Flash.

2. Current trends in Planar Technology

2.1 CMOS

One may argue that the steep increase of the number of transistors on a chip went too fast to cope with. A common notion in this respect is the "design gap" (or productivity gap). More and more transistors can be produced, but we lack the manpower to efficiently design all these circuits with so many transistors. Figure 3 illustrates this problem, as it was quantified around the turn of the Century.

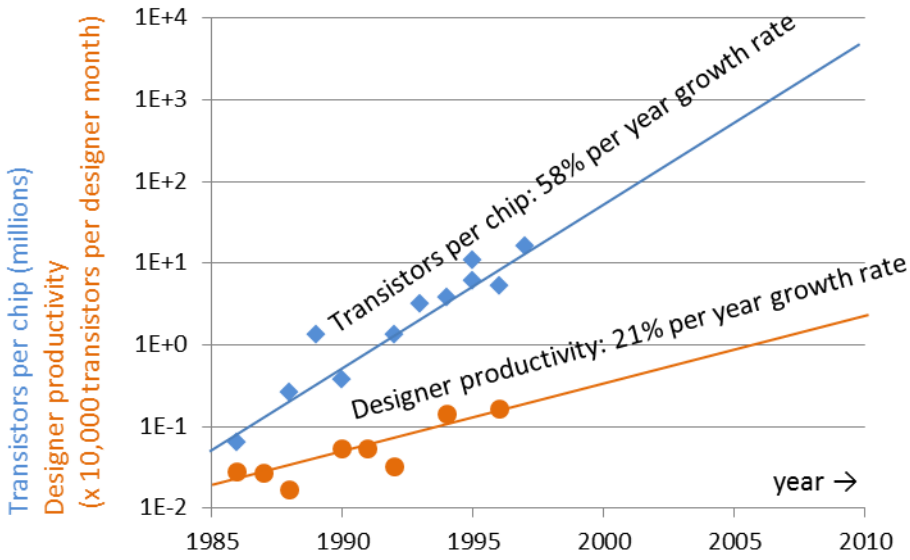

Figure 3: the design gap in microelectronics. More and more transistors can be made in a chip, but the manpower to make the designs is missing; and this issue gets worse over time. The trend lines are derived from data over the period 1986-1997 [8].

While the productivity of integrated circuit designers (expressed in transistors per month) has been estimated to grow with a very respectable 21% per year [8,9], this is significantly outpaced by the transistor count explosion. Inevitably this leads to quick and dirty designs as well as massive re-use of old designs in new chips. Integrated circuits designed with too little manpower tend to be unnecessarily large and power consuming. To indicate the severity of this

problem, it suffices to note that an application-specific circuit (ASIC) is typically a thousand times more energy efficient than a general-purpose microprocessor performing the same task.

Besides design manpower, other bottlenecks in the advancement of computing systems are the relatively slow improvement of memory access time (in particular for DRAM) and the clock frequency limitation mentioned earlier. For low-power computing, important for mobile devices, the reduction of the power supply voltage is presently the most challenging target. Multigate transistors and ultra-thin silicon-on-insulator were recently embraced by industry to facilitate a supply voltage reduction (in 2011 and 2014 respectively). But a further lowering will require disruptive transistor technologies, where off-state leakage is not governed by carrier diffusion. Examples are tunnelling transistors [10,11] and the piezo-FET [12].

The expected slowdown in further miniaturization has led to a reconsideration of the main course of action for the advancement of microelectronics. In particular the use of novel materials is considered to boost the performance of contemporary microchips. In fact, new materials have already been steadily introduced to CMOS in the past period. While conventional CMOS basically consisted of silicon, silicon dioxide and aluminium, these materials are being replaced one by one. In 1997, copper interconnect, using the dual-damascene process, was introduced by major manufacturers to replace aluminium. Around 2007, the silicon dioxide gate dielectric was replaced by hafnium-oxide based materials. In conjunction to that change, the gate material was changed from polycrystalline silicon to metal as well. Source and drain regions were changed from pure (highly doped) silicon to silicon-germanium alloy in the early 2000s.

The one material that did not change in CMOS transistors was in the channel: silicon. However, by creating huge strain (~1 GPa) in this material through fabrication, the material properties were altered considerably. Most notably the mobility of electrons and holes was improved by this strain engineering, which found its way to mass manufacturing around 2003 [13].

Contemporary research in CMOS involves the study of silicon replacement by materials with even higher electron and hole mobilities. As higher mobility means lower resistance, such materials can enable lower-power transistors. Inconvenient as it is, no semiconducting material is known to outperform silicon in terms of *both* carrier mobilities[3]. Compared to silicon, several semiconductors offer a higher electron mobility. As channel material for the NMOS transistor, the best candidate today is InGaAs. Higher hole mobilities than found in strained silicon are rare. The most likely candidates for the PMOS channel are germanium, or GeSn alloy. Hundreds if not thousands of researchers and engineers are developing techniques to produce CMOS with channels of these new materials, with promising results being reported [15,16].

The emergence of a mature manufacturing platform for new semiconductors such as InGaAs and Ge offers attractive new possibilities for particle detector R&D, as will be discussed in more detail in Section 3. However, first we take a broader look at planar technology beyond CMOS integrated circuits.

[3]Graphene does show higher electron and hole mobilities than silicon, but has no bandgap, which complicates the realization of a competitive transistor using this material. Many pursue the opening of the graphene bandgap (see e.g. [14]). In practice band gap formation in graphene comes hand in hand with a steep decrease in carrier mobility.

2.2 Memory technology

Solid-state memories have evolved as quickly as CMOS technology since their market introduction in 1970 [3,17]. In fact, in recent years memory chips contain finer detail than CMOS chips. But largely, the progress in these technologies goes hand in hand. For CMOS and stand-alone memory chips such as DRAM and Flash, the starting material is monocrystalline silicon. The manufacturing toolset is almost the same. Nevertheless, some recent advances deserve special mention at this point.

It is recognized in the field that the diversity in memory technologies is a handicap for system designers. Ideally one would prefer a memory combining the best properties of existing memories: high speed, non-volatility, low switching energy and high write endurance [18]. Not only would a single-memory system be easier (and cheaper) to design and produce. The power consumption will decrease as less data would be transported from one memory to another.

Hence, researchers are on a quest for a non-volatile memory technology with a performance superior to Flash. And indeed, several attractive alternative technologies emerge [19]. Figure 4 presents the four main contenders for non-volatile data storage on a chip. These new technologies outperform Flash in terms of read and/or write bandwidth; endurance is also better in most reports. Further, radiation hardness is much better for some of memory types, in particular magnetic RAM and ferro-electric RAM; see [20] and references therein for more information. But as the graph indicates, these contenders cannot yet compete in terms of storage capacity, and therefore, price.

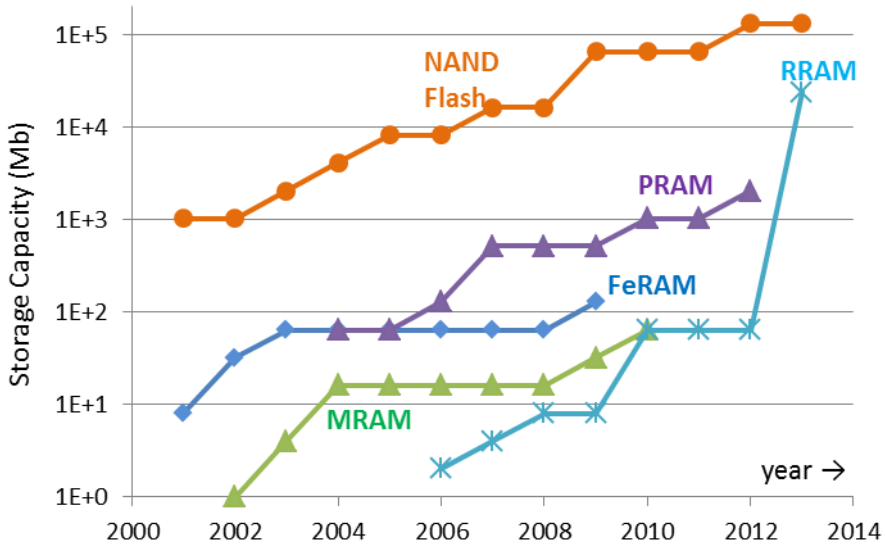

Figure 4: Number of bits per chip for several competing non-volatile solid-state memories. NAND Flash is leading, both in market share and in storage capacity. However, several contenders have appeared lately, classified by the principle of information storage: FeRAM (ferro-electric RAM), MRAM (magnetic RAM), PRAM (phase-change RAM), and most recently RRAM (resistive RAM). Data adopted from [21].

2.3 Other planar technologies

While microelectronics evolved rapidly, the newly developed planar-technology fabrication techniques were adopted in many adjacent fields, and expanded for different applications. Flat-panel displays, photovoltaics, light-emitting diodes (LEDs) and semiconductor lasers are the most prominent of a wide range of technologies relying on microfabrication techniques. Usually, a starting substrate different from monocrystalline silicon is used, such as glass, a III-V semiconductor or sapphire. But in these application domains, similar techniques are used to form and pattern microscopic structures of material on one side of the substrate. A broad range of additional techniques was developed specifically for these devices such as screen-printing, freeze-drying, and rubbing. For reviews of these technologies, we refer the reader to [22-27].

In the context of Technology and Instrumentation for Particle Physics, the topic of these conference Proceedings, it is important to realize that semiconductors other than silicon are rapidly gaining interest by both academic and industrial research teams. In particular, new developments in LED lighting, power transistor technology and photovoltaics will be covered in this section.

In the past few years, LED lighting has rapidly penetrated the consumer market. At the basis of this disruptive technology shift lies the development of gallium nitride technology, enabling high-efficiency blue and (indirectly) white-light emission. Monocrystalline GaN, a III-V semiconductor, has been notoriously difficult to produce with good quality. Long-term research programs at Nichia Corporation and Nagoya University led to important breakthroughs in GaN growth and doping.

GaN thin films for LEDs are grown epitaxially on sapphire or silicon-carbide substrates. Although the techniques are now well mastered, the price of GaN wafers is very high compared to silicon, which limits the applicability of GaN technology for other purposes. In particular, GaN attracts huge research interest from the power electronics community for its superior performance to silicon in this domain. It is considered likely that cheaper approaches are soon deployed for GaN growth, such as GaN-on-silicon [28,29]. Similarly, silicon carbide (SiC) is highly attractive for its materials properties, but substrate cost prohibits widespread research and application. For the state of the art of SiC and GaN power transistors, see e.g. [30].

For photovoltaics, thin-film semiconductors are actively studied as a possible replacement for bulk silicon solar cells. Thin-film photovoltaic panels require relatively little production energy, while this is considered a bottleneck for the further production upscaling of bulk silicon photovoltaics. Considerable effort has therefore been put in the development of thin-film photovoltaic technologies, in particular with amorphous-silicon (a-Si), CdTe, and CIGS (copper-indium-gallium-selenide) semiconductors for photoelectric conversion. It is difficult in practice to gain market share against the established silicon PV market, as explained for instance in [31]. But still, a-Si, CdTe and CIGS solar panels have reached respectable market shares in the recent past, illustrating that the technology to mass manufacture these semiconductor devices with high yield at low cost is mature.

Of these three technologies, CIGS is of particular interest to the Particle Physics community. Reportedly, CIGS solar cells outperform all other photovoltaic technologies in

terms of radiation hardness. We refer the reader to the excellent overview in [32] for further information. In essence, the radiation hardness of the material is attributed to self-repair mechanisms related to the high diffusion of copper.

3. The emergence of new semiconductors: prospects for radiation imaging

The semiconductor device community is quickly broadening scope in recent years, moving away from the traditional focus on silicon and GaAs to other semiconductors. The fabrication technology of GaN, InGaAs and Ge devices is maturing, and the substrates are becoming better-quality, larger in size and less expensive over time. As the research focuses on electronic devices, only a thin surface layer of the semiconductor of interest is necessary – typically of the order of a micrometre or less. High-energy particle detection with such thin monocrystalline layers may be difficult in view of the low primary ionization charge. It is perhaps necessary to resort to avalanche-mode operation to reach acceptable signal-to-noise ratios in detectors made from these materials.

Thin-film photovoltaic technology offers somewhat thicker semiconductor films in the few-micrometre range, be it of polycrystalline nature. A great advantage of photovoltaic manufacturing technology is its large-area, low-cost approach. Various groups investigate photovoltaic systems-on-foil, a technology that could offer extremely low-radiation length semiconductor junctions, an attractive feature for particle tracking. Alternatively, the photovoltaic technology may be transferable directly to a CMOS pixel readout chip, as has been shown for a-Si and CIGS [33-36].

As the technology of these new semiconductors is now readily available, the question to be answered is, if we can achieve appreciable signal-to-noise ratios from minimum ionizing particles with a well-designed pixel or strip architecture. This would open the way to a new class of radiation-hard, low-radiation length tracking detectors.

References

[1] R. N. Noyce, *Microelectronics*, Scientific American, 237 (3) pp. 62–69 (1977).

[2] J. S. Kilby, *Turning potential into realities: the invention of the integrated circuit*, Nobel Lecture, December 8, 2000.

[3] Images courtesy of Computer History Museum. See http://www.computerhistory.org/semiconductor/timeline/ for background information and more examples.

[4] G. E. Moore, *Cramming more components onto integrated circuits*, Electronics 38(8) 1965.

[5] G. E. Moore, *Progress in digital integrated electronics*, IEEE International Electron Device Meeting, Technical Digest, pp. 11-13 (1975).

[6] Wikipedia: English entry on "Transistor Count" – data of June 2014, and references therein.

[7] International Technology Roadmap for Semiconductors, 2013 Edition, available: http://public.itrs.net .

[8] Semiconductor Industry Association. *International Technology Roadmap for Semiconductors: 1999 edition*. Austin, TX: International Sematech, 1999.

[9] M. J. Flynn and P. Hung, *Microprocessor design issues: thoughts on the road ahead*, IEEE Micro, May-June 2005, pp. 16-31.

[10] A. M. Ionescu and H. Riel, *Tunnel field-effect transistors as energy-efficient electronic switches*, Nature, vol. 479, pp. 329-337 (2011).

[11] A. C. Seabaugh and Q. Zhang, *Low-voltage tunnel transistors for beyond CMOS logic*, Proc. of the IEEE, 98 (12) pp. 2095-2110 (2010).

[12] T. van Hemert and R. J. E. Hueting, *Piezoelectric strain modulation in FinFETs*, IEEE Trans. El. Dev. 60 (10) pp. 3265-3270 (2013).

[13] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. Mclntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson and M. Bohr, *A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors*, IEEE International Electron Device Meeting, Technical Digest pp. 978-980 (2003).

[14] S.Y. Zhou, G.-H. Gweon, A.V. Fedorov, P.N. First, W.A. De Heer, D.-H. Lee, F. Guinea, A.H. Castro Neto, and A. Lanzara, *Substrate-induced bandgap opening in epitaxial graphene*, Nature Materials 6 (10) pp. 770-775 (2007).

[15] B. Duriez et al., *Scaled P-Channel Ge FinFET With Optimized Gate Stack and Record Performance Integrated on 300mm Si Wafers*, IEEE International Electron Device Meeting, Technical Digest, paper 20.1 (2013).

[16] J. A. del Alamo, D. Antoniadis, A. Guo, D.-H. Kim, T.-W. Kim, J. Lin, W. Lu, A. Vardi, and X. Zhao, *InGaAs MOSFETs for CMOS: Recent Advances in Process Technology*, IEEE International Electron Device Meeting, Technical Digest, paper 2.1, 2013.

[17] R. H. Dennard, *Field-effect transistor memory*, U. S. Patent 3,387,286 (Filed July 14, 1967).

[18] S. Åkerman, *Toward a universal memory*, Science 308, 508 (2005).

[19] Y. Fujisaki, *Review of emerging new solid-state non-volatile memories*, Jap. J. Appl. Phys. 52 040001 (2013).

[20] S. Gerardin and A. Paccagnella, *Present and future non-volatile memories for space*, IEEE Trans. Nucl. Sci. 57 (6) 3016 (2010).

[21] K. Zhang, *ISSCC Memory Trends*, Press Kit, IEEE International Solid-State Circuits Conference 2013.

[22] M. D. Archer and R. Hill (eds.), *Clean electricity from photovoltaics*, Imperial College Press 2001.

[23] K.-H. Kim and J.-K. Song, *Technical evolution of liquid crystal displays*, NPG Asia Mat. 1 (1) 29-36 (2009).

[24] Y. Yamamoto, *Technological innovation of thin-film transistors: technology development, history, and future*, Jap. J. Appl. Phys. 51 (2012) 06001.

[25] M. G. Craford, R. D. Dupuis, M. Feng, F. A. Kish, J. Laskar (Eds.), *The 50th anniversary of the LED: An ultimate lamp*, Proceedings of the IEEE, 101 (10), 2013.

[26] R. D. Dupuis and M. R. Krames, *History, development, and applications of high-brightness visible light-emitting diodes*, J. Lightwave Technol. 26 (9) 1154-1171, 2008.

[27] M. J. Madou, *Fundamentals of Microfabrication*, CRC Press 2002.

[28] B. De Jaeger, M. Van Hove, D.Wellekens, X. Kang, H. Liang, G. Mannaert, K. Geens, and S. Decoutere, "*Au-free CMOS-compatible AlGaN/GaN HEMT processing on 200 mm Si substrates*, in Proc. Int. Symp. Power Semicond. Devices, 2012, pp. 49–52.

[29] C. Bayram, J. A. Ott, K.-T. Shiu, C.-W. Cheng, Y. Zhu, J. Kim, M. Razeghi, and D. K. Sadana, *Cubic phase GaN on nano-grooved Si (100) via maskless selective area epitaxy*, Adv. Funct. Mater. 2014, DOI: 10.1002/adfm.201304062.

[30] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, *A survey of wide bandgap power semiconductor devices*, IEEE Trans. Power Electron. 29 (5) 2155 (2014).

[31] R. M. Swanson, *A vision for crystalline silicon photovoltaics*, Prog. Photovolt: Res. Appl. 14 pp. 443–453 (2006).

[32] J.-F. Guillemoles, L. Kronik, D. Cahen, U. Rau, A. Jasenek, and H.-W. Schock, *Stability issues of Cu(In,Ga)Se_2-based solar sells*, J. Phys. Chem. B, 104, pp. 4849-4862 (2000).

[33] A. Franco, Y. Riesen, M. Despeisse, N. Wyrsch and C. Ballif, *High spatial resolution of thin-film-on-ASIC particle detectors*, IEEE Trans. Nucl. Sci. 59 (5) 2614 (2012).

[34] J. Lu, A. Y. Kovalgin, K. H. M. van der Werf, R. E. I. Schropp and J. Schmitz, *Integration of Solar Cells on Top of CMOS Chips Part I: a-Si Solar Cells*, IEEE Trans. El. Dev.58 (7) pp. 2014-2021 (2011).

[35] J. Lu, W. Liu, A. Y. Kovalgin, Y. Sun, and J. Schmitz, *Integration of Solar Cells on Top of CMOS Chips—Part II: CIGS Solar Cells*, IEEE Trans. El. Dev. 58 (8) pp. 2620-2627 (2011).

[36] O. Matsushima, K. Miyazaki, M. Takaoka, T. Maekawa, H. Sekiguchi, T. Fuchikami, M. Moriwake, H. Takasu, S. Ishizuka, K. Sakurai, A. Yamada, and S. Niki, *A high-sensitivity broadband image sensor using CuInGaSe_2 thin films*, IEEE International Electron Device Meeting, Technical Digest, Dec. 2008, pp. 11.2.1–11.2.4.