

## Recent Achievements of the ATLAS Upgrade Planar Pixel Sensors R&D Project

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The ATLAS experiment plans to introduce an all-silicon inner tracker with the HL-LHC upgrade to cope with the elevated occupancy. With silicon, the occupancy can be adjusted by using the unit size (pixel, strip or short strip sensors) appropriate for the radiation environment. For radiation damage reasons, only electron-collecting sensor designs are considered (n-in-p and n<sup>+</sup>-in-n). Beyond a fluence of about  $10^{15} \text{ n}_{eq} \text{ cm}^{-2}$ , trapping becomes the dominant radiation effect and electrons are trapped significantly less than holes.

To investigate the suitability of pixel sensors using the proven planar technology for the upgraded tracker, the ATLAS Planar Pixel Sensor RD Project was established. Main areas of research are:

- performance assessment and improvement of planar pixel sensors at HL-LHC fluences
- the achievement of slim or active edges to provide low geometric inefficiencies without the need for shingling of modules

It has been demonstrated with sensors from different vendors that planar pixel sensors can be operated and still yield more than 5000 electrons of signal charge even above  $10^{16} \text{ n}_{eq} \text{ cm}^{-2}$ ; hit efficiencies of well above 97% were obtained.

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## 1. Planned ATLAS upgrades

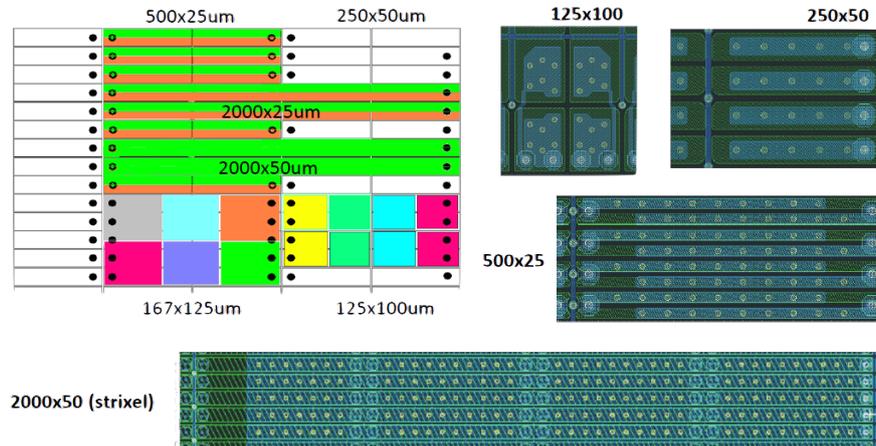
To extend the physics reach of the LHC, upgrades to the accelerator are planned to increase the peak luminosity up to possibly  $(5-8) \cdot 10^{34} \text{cm}^{-2} \text{s}^{-1}$  which will enable the experiments to collect up to  $3000 \text{fb}^{-1}$  of data [1]. It is foreseen to upgrade the accelerator chain in three long shutdowns (LS1, LS2 and LS3). This, however, will lead to increased occupancy and radiation damage of the inner trackers, approaching fluences of a few  $10^{16} \text{n}_{eq} \text{cm}^{-2}$  at the innermost layer and still some  $10^{15} \text{n}_{eq} \text{cm}^{-2}$  at the outer pixel layers.

The ATLAS experiment plans during each of the shutdown periods upgrades to the detector. The ATLAS pixel detector is composed of  $250 \mu\text{m}$  thick n-in-n pixel sensors with cell sizes of  $50 \times 400 \mu\text{m}^2$  and connected to 16 readout chips of the FE-I3 generation [2]. During the ongoing shutdown LS1 a new fourth pixel layer have been installed, the so called Insertable b-Layer (IBL) [3]. The pixel size for the IBL was shrunk down to  $50 \times 250 \mu\text{m}^2$ . The radiation tolerance was rated and tested up to a fluence of  $5 \cdot 10^{15} \text{n}_{eq} \text{cm}^{-2}$ . On the readout side a new readout generation was developed, the FE-I4 chip.

For the phase II shutdown LS3, foreseen for the years 2022 and 2023, a complete replacement of the ATLAS inner tracker is planned.

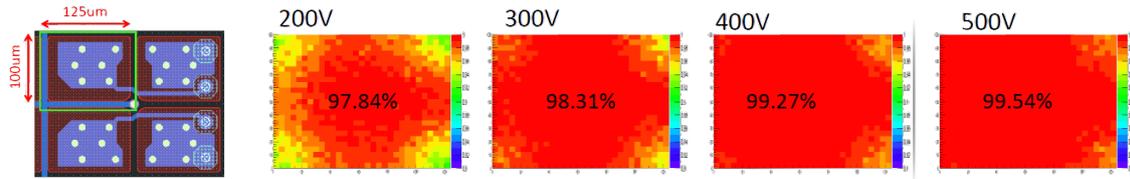
## 2. New Pixel Sizes and Designs

The use of pixel geometries optimized for normal incidence tracks leads to degradation in the tracking performance at larger angles that can be mitigated by varying the sensor pixel geometry in different parts of the pixel array. Alternative pixel geometries (shown in Fig.1) have all been designed to be compatible with the FE-I4 readout chip which has a pitch of  $50 \times 250 \mu\text{m}^2$ .

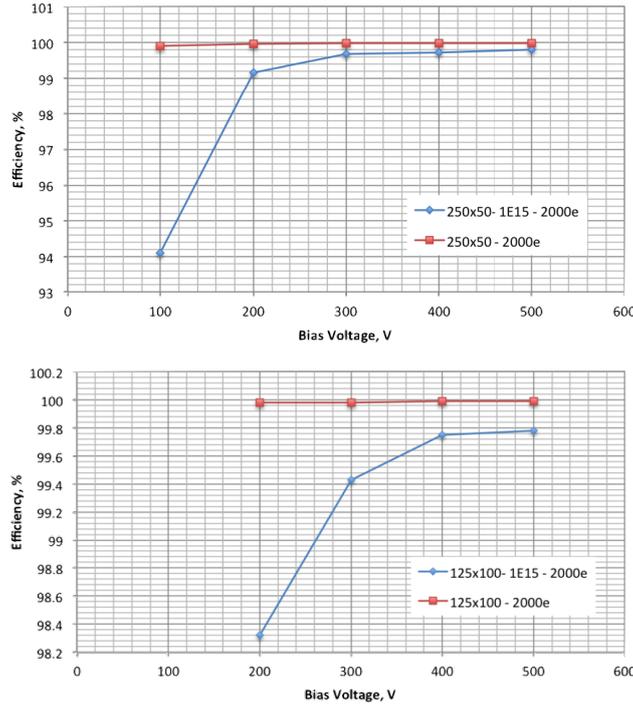


**Figure 1:** Various n-in-p pixel sizes, punch trough/polysilicon, AC and DC coupled [4]

These pixel geometries have been investigated before and after irradiation in PPS testbeams. The efficiency results are shown in Fig.2 and Fig.3. The results show a good efficiency and the sensors perform as expected.



**Figure 2:** Pixel efficiency of an irradiated ( $1 \cdot 10^{15} n_{eq} cm^{-2}$ ) Single Chip Assembly at different bias voltages [4]



**Figure 3:** Efficiency measurements at DESY testbeam. **Top:** Single Chip Assembly with  $250 \times 50 \mu m^2$  pixel size, **Bottom:** Single Chip Assembly with  $125 \times 100 \mu m^2$  pixel size.[4]

### 3. Radiation Hardness

To reproduce the realistic conditions in the experiment planar pixel silicon sensors are irradiated with various particle types and energies. Fig.4 shows the charge collection efficiency of  $n^+$ -in-n FE-I3 based single chip assemblies. They were irradiated up to  $2 \cdot 10^{16} n_{eq} cm^{-2}$  and still show satisfactory results in laboratory and testbeam measurements.

The measurements of the n-in-p sensors, shown in Fig.5, show also a good charge collection efficiency after a fluence of  $1.4 \cdot 10^{16} n_{eq} cm^{-2}$ , irradiated with 800 MeV protons.

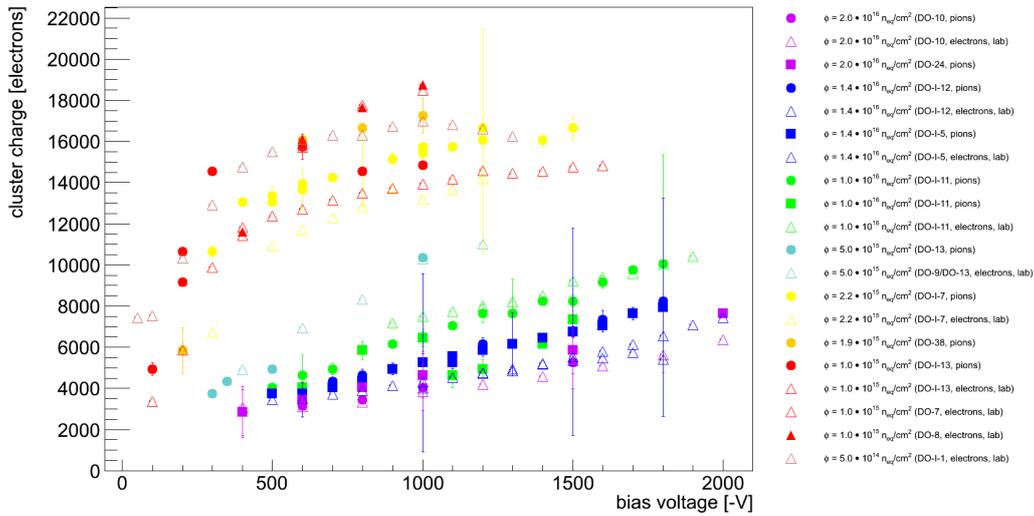


Figure 4: Charge collection vs. bias voltage of several irradiated n<sup>+</sup>-in-n FE-I3 Single Chip Assemblies [5]

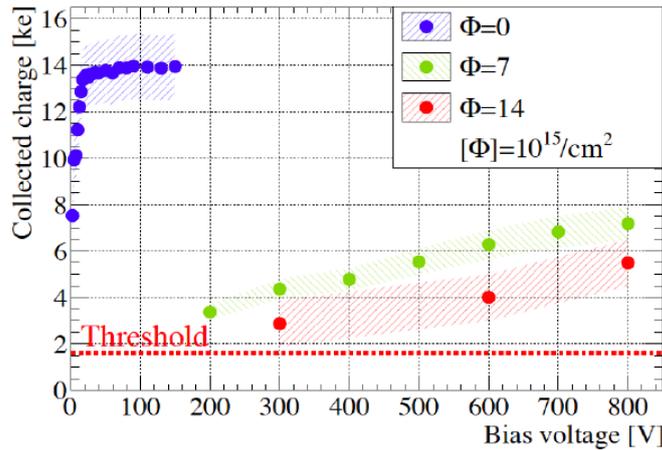


Figure 5: Charge collection vs. bias voltage of several irradiated n-in-p FE-I4 Single Chip Assemblies [6]

#### 4. Conclusion and Outlook

The planar pixel sensors are a well understood and proven technology. The PPS group has demonstrated that the sensors are well suited even at phase II fluences of  $2 \cdot 10^{16} n_{eq} cm^{-2}$ . New pixel designs have been realized and successfully tested.

The PPS community shows promising approaches to fulfill the expected phase II requirements.

#### References

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