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High-Resolution and Low Resource Time To Digital Converters for the KM3NeT Neutrino Telescope

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Precise measurements on time intervals (TIs) are frequently needed in many physics applications such as particle detection. Time to Digital Converters (TDCs) perform conversion of TIs into a digital word. In the case of KM3NeT, thirty-one TDCs are used to discretize the photomultiplier output. Both the event width and the occurrence time require an accuracy of 1 ns. An oversampling technique has been used to achieve this resolution. The proposed TDC readout is based on a Field-Programmable Gate Array (FPGA) Xilinx Kintex-7 with low resource occupancy and controlled by embedded Lattice Mico LM32 processor.

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1.Introduction

The sensitive elements of a neutrino telescope are the optical detectors, which in the case of KM3NeT are the small photocathode area photomultipliers (PMT) distributed inside a glass sphere to form the Digital Optical Module (DOM) [1]. Each DOM has 31 small PMTs that collect the Cherenkov light and convert it into electronic signals. In order to translate these signals into the arrival time of the photons, they are processed by Time to Digital Converters implemented on a Kintex-7 FPGA.

2.KM3NeT Requirements

The raw data from the PMTs consist of a continuous series of hits that should be digitized. Each hit corresponds to an analogue pulse of a signal that passed a preset threshold. The digital data correspond to the timestamp and length of the time-over-threshold signal that is produced by the active base of each PMT. The timestamp corresponds to the time when the leading edge of the signal crossovers the threshold, and the length is the time difference between the leading and trailing edges. Both, timestamp and length of pulse, require an accuracy of 1 ns.

3. 4-Oversampling Technique

Oversampling method uses a sampling frequency significantly higher than twice the bandwidth (or highest frequency) of the signal being sampled. For the KM3NeT readout system, the “significantly higher” sampling frequency is obtained using different edges of multiple phase-shifted clocks. This method is called asynchronous oversampling because the clocks used to create the sampling frequency are nominally equal to the data stream accuracy 1 ns [2]. The function of the two extra clocks combination is shown in Figure 1.

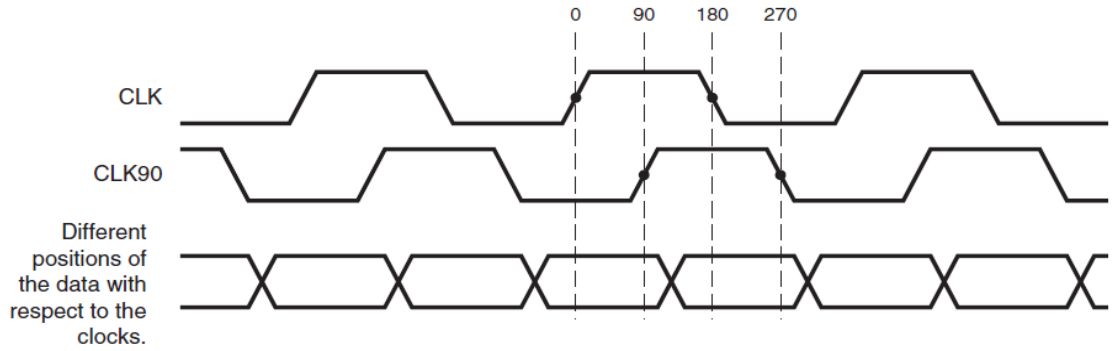

Figure 1: Oversampling technique using two phase-shifted clocks.

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4.Implementation

A 31 channel TDC has been designed in a Xilinx Kintex-7. Because of the programmable characteristic of an FPGA, a TDC readout implemented in this device has flexible characteristics. Here, a simplified TDC is designed to verify the idea of deserializing the raw data by means of dedicated input/output blocks of the FPGA [3]. The CLB board provides small quartz of 25 MHz, the clock signal is first transferred from a clock pin to a buffer in the centre of the FPGA, and then fanned out to the inner PLLs to provide two high frequency clocks of 250 MHz and 90° phase shifted. 4-Oversampling method increases the sampling frequency up to 1 GHz achieving the desired accuracy of 1 ns. TDC implementation is shown in Figure 2.

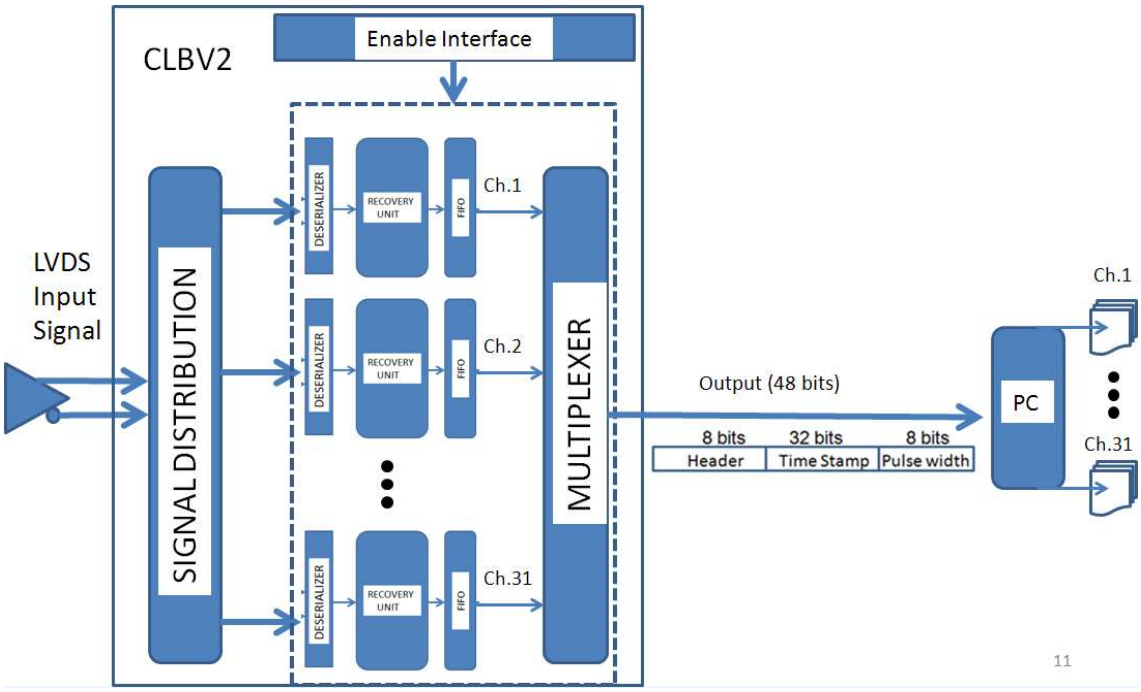

Figure 2: TDC readout system architecture implemented in a Kintex-7.

5. Results

Two different well-known patterns have been created to test the TDC implementation using an external generator based on Virtex-6 FPGA. Pattern-1 has four different width pulses of 10, 25, 35 and 40 ns. Pattern-2 has two different width pulses of 25 and 40 ns. Both, pattern-1 and pattern-2, are replicated 5000 times and sent to the TDC readout system through a Xilinx FMC Debug board. The pulse trains are oversampled by deserializer blocks and computed by

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additional firmware based on Kintex-7 FPGA technology. The results are stored in FIFO memory and sent to the computer via serial communication using a Lattice LM32 embedded microprocessor. Figure 3 shows the results of the data analysis.

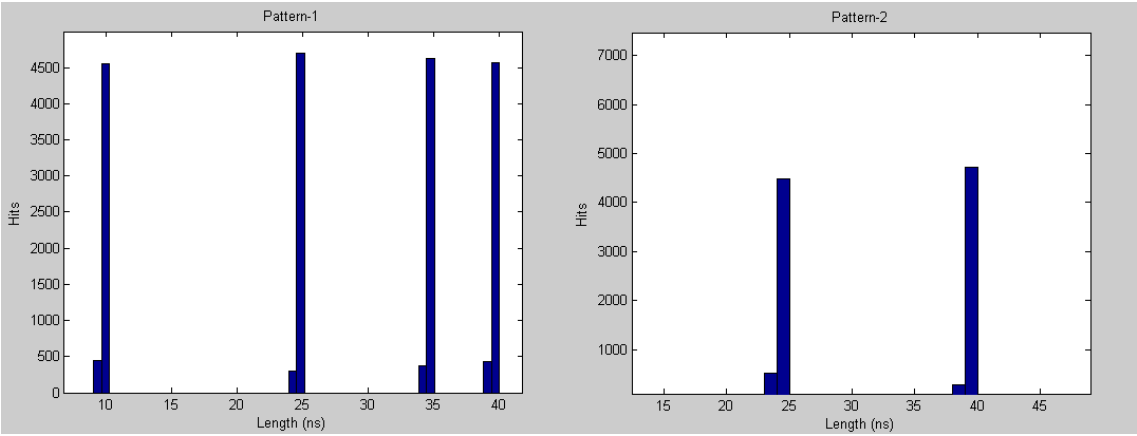

Figure 3: Test results for two raw data patterns, computed by the TDC readout system.

6. Conclusions

1 ns Time to Digital Converter designed for KM3NeT has been implemented using deserializer primitives, within the input/output blocks of Kintex-7 FPGA, working in oversampling mode. 4-Oversampling technique using two high frequency clocks of 250MHz has been designed to achieve a resolution of 1 ns. The TDC readout system has been tested using an external pattern generator based on Virtex-6 and Kintex-7 FPGA

7.References

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[3]. U.Guin “Design for bit error rate estimation of high speed serial links” VLSI Test Symposium (VTS), 2011 IEEE 29th. pp 278-283

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