

Digital Optical Module Read-Out Electronics System of the KM3NeT Neutrino Telescope

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on behalf of the KM3NeT collaboration

The KM3NeT collaboration aims at the construction of a neutrino telescope with a volume of several cubic kilometres at the bottom of the Mediterranean Sea. The telescope will consist of an array of Digital Optical Modules that will detect the Cherenkov light originated by the interaction of the neutrinos in the proximity of the detector. In this contribution the main components of the read-out electronics of the Digital Optical Module, are described: the Photomultiplier Tube bases, in charge of converting the analogue signal produced by the 31 3" Photomultiplier Tubes into a Low Voltage Digital Signal; the Octopus boards, that transfer the Low Voltage Digital Signals from the Photomultiplier Tube bases to the Central Logic Board; the Central Logic Board, the most complex board of the read-out system, hosting 31 Time-to-Digital Converters with 1 ns resolution and the White Rabbit protocol embedded in the Central Logic Board Field Programmable Gate Array; the Power Board, which delivers all the power supply required by the DOM electronics.

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1.Introduction

KM3NeT is a future European research facility in the Mediterranean Sea that will house a neutrino telescope of cubic kilometer scale. Cherenkov light from neutrino-induced secondary particles will be detected by an array of Digital Optical Modules (DOM) consisting of high pressure resistant glass spheres hosting photomultipliers inside. This vessel is called the Digital Optical Module (DOM) and it is composed of 31 small 3 inch photomultipliers (PMTs) distributed around the glass sphere, which collects the Cherenkov photons and transform them into electronic signals. The PMTs are suspended in a foam support structure: 19 in the lower hemisphere and 12 in the upper hemisphere. Each PMT has its own adjustable high voltage supply integrated in the PMT base. In addition to the PMTs the DOM contains a printed circuit board, the Central Logic Board (CLB), which converts the electronic signals from the PMTs into time, pulse duration and identification information in the Time To Digital (TDC) core embedded in the Field Programmable Gate Array (FPGA) of the CLB. The CLB integrates the White Rabbit Protocol (White Rabbit is a fully deterministic Ethernet-based network for general purpose data transfer and synchronization), which allows to synchronize the all the KM3NeT DOMs within 1 ns resolution. The data provided by the PMT bases is collected and distributed to the CLB by means of two boards (one for each hemisphere), the so called Octopus Boards. It also contains the electronic and photonic components for an optical serial link to the shore. All necessary DC power is provided by the Power Board (PB). An aluminium structure provides heat conduction between the electronics inside and the exterior of the sphere. In this contribution all components (CLB, PB, Octopus and PMTs) of the readout electronics of the DOM are described.

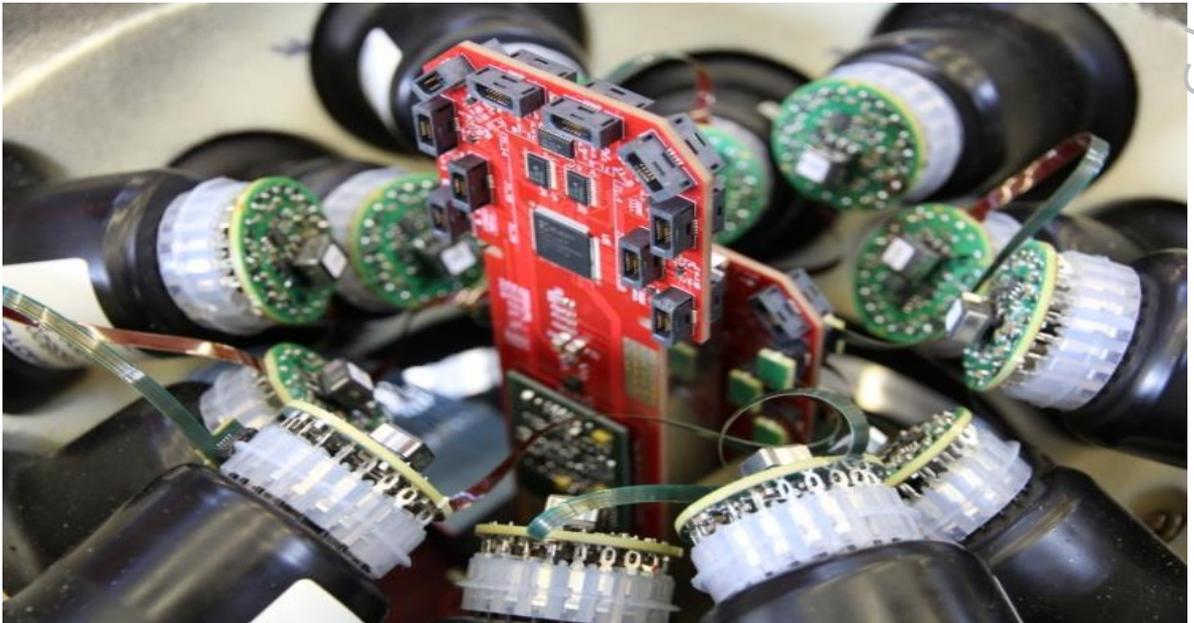


Figure 1: Half DOM open: View of the PMT bases (in green) and the Octopus boards (in red)

2.Photo Multiplier Base

The PMT base is in charge of discretizing the signal read by the PMT and to provide the High Voltage (HV) for the PMT. The PCB contains a pre-amplifier, a comparator (Time over Threshold) and identification identifier. Every PMT must give the same output signal when it is hit by a single photon. The gain of a PMT depends on the supplied high voltage. The HV for each PMT is individually adjustable from 800 to 1400 V. Consequently each PMT gets its own HV circuit board. I2C protocol is used to be able to control the PMT base and to change the HV. The power consumption of each PMT base is around 4.5 mW. An additional function of the PMT base is the digitisation of the analogue output signal of the PMT. The output signal is converted from a charge signal to a voltage signal, followed by a conversion to a digital level by a comparator, resulting in a Time Over Threshold (TOT) signal. The comparator can be adjusted to the required TOT value using I2C protocol. The TOT signal is transferred to the DOM logic by a LVDS connection.

3.Octopus Board

Within each hemisphere, the LDVS signals from the PMT bases are collected on a custom electronics board (Figure 1), called the Octopus board, and transferred to the DOM central logic board. The boards also provide connection for the electrical power to the PMT bases and the I2C communication control. For each PMT, the electrical power can be switched on/off individually by the slow control and in case of overload of a PMT the power will be switched off automatically. This can be monitored by the Fault Flag (FFLG). A clock enabled signal to the PMTs for the I2C communication avoids digital interference.

4.Power Board

For an efficient transfer of the electrical power the voltage level must be high and the current low, because of the power loss depends on I^2R of the cable. In addition, the different electronic of the DOM require many different voltage levels for their performance. Therefore, the power conversion board inside the DOM (PB) derives all different client voltage levels from an input voltage of 12 V. Modern Converters at high frequency are used to obtain a high efficiency power conversion. To protect the other electronics inside the DOM against possible high frequency noise interference, the converter board is located in a shielded part of the cooling mushroom. On the other hand, where the cooling of the board will be more efficient at this location

5. Central Logic Board

The DOM Central Logic Board (CLB) is the main electronic board in the readout chain of KM3NeT. The LDVS signals generated by the PMT bases and collected and distributed by the Octopus boards arrive at the CLB where they are discretized by means of 1 ns resolution TDCs. The TDC data is sent on-shore after being organized and timestamped at the CLB. In order to synchronize the DOMs in KM3NeT, the CLB integrates the White Rabbit Protocol that provides a global time for KM3NeT with 1 ns resolution. The CLB takes care also of the read-out of several instruments, as it is the case of the Compass, Tiltmeter and Temperature sensors, all of them integrated on the same CLB PCB, the Piezo, the Nanobeacon and the Acoustic Hydrophone. The main component of the CLB is a Kintex FPGA. This device, which integrates the TDCs and the White Rabbit Protocol, allows the reconfiguration of the firmware of the CLB. It is feasible to store up to four FPGA images in a SPI memory, three of them reconfigurable. The non-reconfigurable one provides a safe start for the FPGA in case of corruption of the 3 reconfigurable images, being possible to choose to boot the FPGA with any of the four. The Kintex FPGA family is a very low power consumption family being able to have a power consumption on the CLB lower than 4 Watts. In order to reduce the power consumption no operative system is used. Instead the control of the CLB is achieved through a specific embedded software running on a LM32 microprocessor (an open source firmware microprocessor from Lattice). Also the price of the CLB is expected to be reduced when compared with the first version of CLB developed using the minimodule of Virtex 5 FPGA.

6. References

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