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The NA62 LAV front-end electronics and the L0 trigger generating firmware

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The aim of the NA62 experiment is to measure the branching ratio of the decay $K^+ \to \pi^+ \nu\bar{\nu}$ to within about 10%. The large-angle photon vetoes (LAVs) must detect particles with better than 1 ns time resolution and 10% energy resolution over a very large energy range in order to reject the dominant background: photons coming from $\pi^+\pi^0$ decays. A low threshold, large dynamic range, time-over-threshold based solution has been developed for the LAV front end electronics (LAV-FEE). Our custom 32 channel 9U board uses a pair of low threshold discriminators for each channel to produce LVDS logic signals. The achieved time resolution obtained in laboratory, coupled to a readout board based on the HPTDC chip developed at CERN, is ∼100 ps. For LAV-FEE, a FPGA-based level-0 trigger providing slewing-corrected trigger time with similar precision has also been developed.

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1. The readout system of the NA62 large-angle photon vetoes

The aim of the NA62 experiment [1] is to measure the branching ratio of the decay $K^+ \to \pi^+ \nu\bar{\nu}$ to within about 10%. The large-angle veto (LAV) [2] system is designed to detect photons from kaon decays, as well as muons and pions in the beam halo. The veto detectors must provide a time measurement with $\sim$1 ns resolution and an energy measurement with $\sim$ 10% precision. The readout system must discriminate signals with few-millivolt thresholds in order to keep the detection efficiency as high as possible for low-energy photons. The LAV detectors is composed of $\sim$ 2500 lead-glass blocks coupled with photomultipliers (PMT). Due to their $\sim$1ns time resolution and the rise time of the PMT ($\sim$5 ns), the requirements are not stringent on the time measurement. The expected energy deposit in the LAV stations covers a range from $\sim$10 MeV up to $\sim$30 GeV.

The readout for the 12 LAV stations consists of two different types of boards: a front end card (LAV-FEE)[3, 4], and a digital readout board called TEL62 [6], used by most of the NA62 detectors. The LAV-FEE converts the signal coming from the PMT into an LVDS digital signal using two comparators with different thresholds. The duration of the LVDS pulses is equal to the time over a programmed threshold (ToT) of the analog signal. The LVDS signals are sent to the TEL62 board in which a TDC mezzanine [5] produces digital leading and trailing times. The TEL62 on-board FPGAs are used to correct raw hits times and to produce a L0 trigger primitive (see 4) to be sent to the L0 trigger processor. On a positive L0 trigger request the TEL62 sends the data to the L1 PCs through 3 Gbit ethernet interfaces. The LAV system has $\sim$ 2500 input channels and $\sim$ 5000 digital readout channels in total. The system in expected to sustain rates of physical particles up to 100KHz per channel and to produce a data volume of $\sim$2.4 Gbit/s for each stations.

2. The LAV front end electronic board

The LAV-FEE is implemented on a 9U VME standard layout. No VME bus line is connected to the board, only customs $\pm$ 7.5 V power lines are used. The 32 analog inputs are connected to the board using two DB37 connectors (see fig 1). As mentioned before, each single input produces two different outputs. The resulting 64 LVDS digital outputs are connected to the TDC using two SCSI2 connectors. The communication and the threshold setting are managed by the CAN-Open protocol through two RJ-45 connectors. To simplify maintenance and reduce costs the 9U motherboard manages input, output and power distribution while the rest of the functionalities are implemented on 4 types of mezzanine.

The core part of the LAV FEE are the ToT mezzanines, which operate on the analog signal to produce the LVDS output. The LAV FEE board houses 16 of these mezzanines, consisting of 2 input channels each. The MIP signal is expected to be $\sim$12 mV on top of a 2-3 mV noise. Therefore, the ToT system works with an effective threshold, of a 5-6 mV in order to maximize the detection efficiency. To improve signal to noise separation and reduce the walk dependence on the analog amplitude, an amplification of 6 is used. A very low noise, high bandwidth (800 MHz), high speed Current Feedback Amplifier (AD8001) is used for this purpose. The amplified signal sent to two LMH7220 High Speed Comparators with LVDS drivers. These devices compare the input with programmable thresholds which can be adjusted from $\sim$ 4 to $\sim$ 120 mV with a 12-bit DAC in the board controller mezzanine.

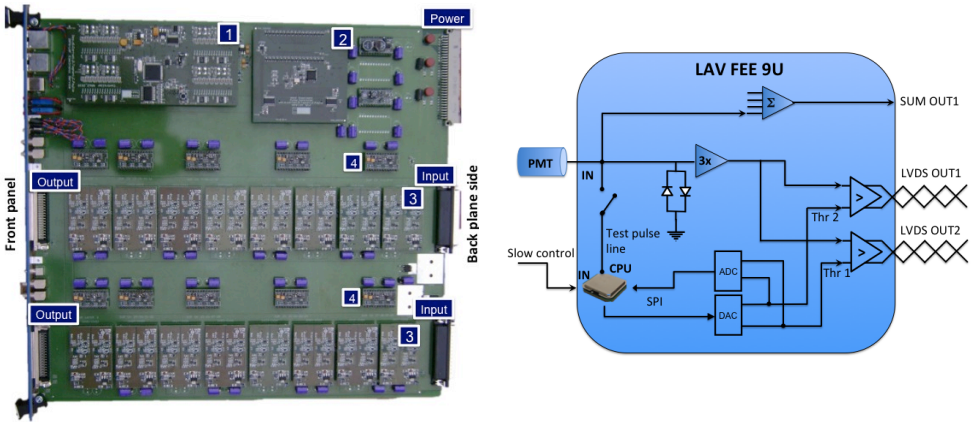

Figure 1: *The LAV front end board (left) and its block diagram (right).*

3. Testing LAV front-end boards

In order to test and characterize all the LAV FEE boards, an automatic test stand has been set up both at Laboratori Nazionali di Frascati (LNF) and at the experimental site at CERN.

3.1 Test setup

A pulse generator (Agilent 81110A) was used to generate test signals having a variable height and a fixed rise time of 5 ns and a fall time of 16 ns. The generated signal was passively split into 32 copies (equal within 2%) and fed into the two input DB37 connectors of one LAV FEE board. The 64 LVDS outputs were connected to a VME commercial board (CAEN V1190B) housing the HPTDC chip, the same TDC ASIC as the NA62 TDCb. Digital data was collected through a VME controller (CAEN V1718) and stored on a PC. The PC was programmed to configure front-end threshold values through USB and the pulse generator through GPIB, changing the signal amplitude in such a way that an automatic procedure was established.

3.2 Test results

Many kind of measurements were performed on the boards: noise, hysteresis, threshold calibration and time resolution. Here we focus on the last two. For the threshold calibration, the amplitude of the input signal and the threshold were varied in the range from 2 mV up to 20 mV. For every configuration the efficiency of each channel was measured as the number of detected pulses divided by the number of delivered pulses. The pulse amplitude corresponding to a certain threshold was chosen as the one for which the efficiency reached 95%. Repeating these measurement for different thresholds, a calibration line was built for every channel. The offset of this line represents the amplitude of the minimum discriminable signal. The distribution of the measured offsets is shown in the left plot in fig. 2. It is clear that the we are able to set a 5 mV threshold in all the channels.

Concerning the time resolution, we performed repeated measurements of the ToT of the input signal. The pulse width is set to a fixed value of (20.00±0.04) ns. The RMS values of the ToT distributions for the all the channels of 80 boards, are represented in the right plot in fig. 2. The

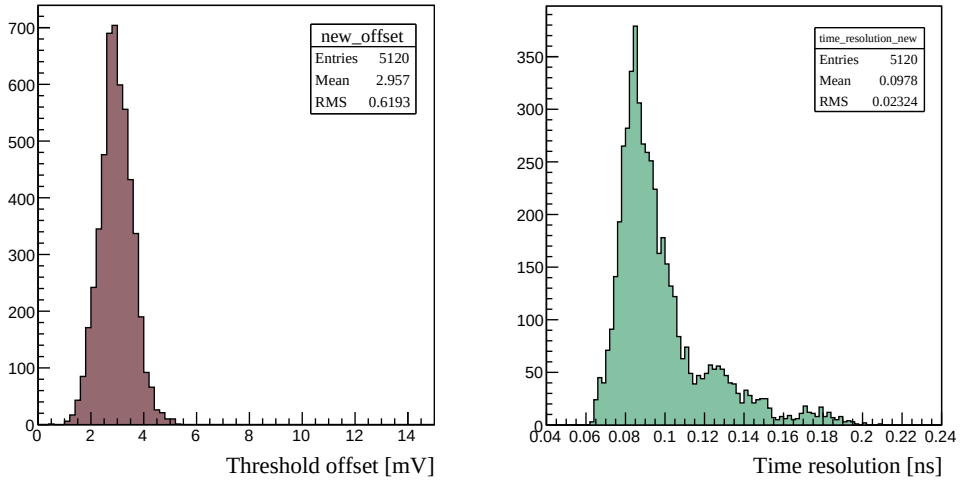

Figure 2: *The distribution of the threshold offsets (left), i.e. the minimum discriminable signal in mV for every channel and the distribution of the RMS of repeated time measurement of a probe signal (right), performed with every channel. The probe signal has amplitude of 100 mV and fixed width of ∼20 ns within 40 ps RMS.*

right tail of the distribution is due to the channels in the last sector of the LAVFEE boards that resulted to be a little more noisy, as they are physically more distant from the power regulators. Nonetheless all the channels have a time resolution better then 200 ps meeting our requirements.

4. LAV trigger-generating firmware

The digital readout of the all the detectors participating to the NA62 experiment is based on the TEL62 board [6] which collects data coming from TDCs and transfers it through 3 Gbit ethernet when a trigger signal is received. Some detectors, including the LAV, must at the same time generate the L0 trigger primitive. To this end, detector-specific firmware must be designed. As far as LAV is concerned, the event on which a trigger primitive must be generated is simply the signal crossing both the high an the low thresholds on the same block. In order to find the events and produce trigger primitives, a LAV-specific trigger generating firmware was developed. It consists of an independent data-stream parallel to the data one. As a first step events are distributed among different FIFOs, one for each high threshold and low threshold channel. While the FIFOs are filled, a finite state machine searches for an event, i.e. for the crossing of high and low threshold in the same block. Once the association is performed, the resulting event time is corrected for the slewing (or time-walk) error by means of: $t = t_{low} - \frac{(t_{high}-t_{low})\cdot t_{low}}{V_{high}-V_{low}}$, where V_{high}, V_{low} are the high, low threshold voltages and t_{high}, t_{low} are the respective crossing times. At last, events occurring within a specific time window (programmable up to ∼25 ns) are grouped together to form a cluster whose time is calculated as the average of single times. Finally, the time values of the clusters are sorted and delivered to the last firmware block to build the trigger primitives and send them to the L0 trigger processor.

5. Conclusions

A low cost, large dynamic range, time-over-threshold based solution has been developed for the LAV front end electronics. An automatic test station has been set up at LNF and CERN and ∼80 boards have been characterized and are now up and running at the NA62 experimental site. The achieved time resolution has been measured to be of the order of 100 ps for most of the electronic channels, while the minimum effective threshold has been proven to be less than 5 mV. The LAV-specific primitive-generating firmware has been developed and tested on the TEL62 boards with promising results.

References

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