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RD53 Collaboration and CHIPIX65 Project for the development of an innovative Pixel Front End Chip for HL-LHC

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Pixel detectors at HL-LHC experiments will be exposed to unprecedented level of radiation and particle flux. This paper describes the program of development of an innovative pixel chip using a CMOS 65nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. The RD53 collaboration effort is described together with the CHIPIX65 INFN project.

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The HL-LHC accelerator will constitute a new frontier for the particle physics after the year 2024, once LHC Phase 0 and Phase 1 will be finished, allowing to accumulate an integrated luminosity ten times larger than before. The ATLAS and CMS experiments are facing new experimental challenges, having to distinguish rare events superimposed to more than hundred pile-up events and to cope with much higher particle fluxes. The overall performance of the experiments have to be maintained or even improved in order to exploit the potential of the HL-LHC run. The pixel detector is a fundamental component of the experiment, determining the seed of particle tracking and measuring all primary vertices and impact parameters. Being the closest detector to the beam, a substantial innovation is needed in order for the pixel detector to be well performing in the HL-LHC hostile conditions and survive the whole Phase 2 period.

1. State of the art in HEP and new pixel specifications

Hybrid pixel ASICs in the current LHC experiments can sustain pixel hit rates of up to 200 MHz/cm^2 with an effective resolution of the order of ten microns. An extensively used CMOS 250 nm technology employing a special layout approach (enclosed transistor layout) has been used to implement pixel chips that can survive radiation levels of up to 1 MGy and 10^{14} neutrons/cm^2. For comparison, radiation tolerant ASICs used for space applications can only work at radiation levels up to about 1 kGy.

Recent pixel developments based on CMOS 130nm technology are Velopix[1], Timepix[2], ToPix[3] and the FEI4 chip[4]. The latter has been specified to meet more extreme conditions foreseen for the Phase 1 upgrade of LHC, foreseen for the year 2018. The FE-I4 can be considered as a second-generation LHC pixel detector.

For the HL-LHC period, a new pixel detector will be needed for ATLAS and CMS since the instantaneous luminosity will be more than twice that of Phase 1, reaching 5 10^{34} cm^{-2}s^{-1}, and determining a pile-up of at least 100, for an integrated luminosity of 270 fb^{-1} per year, equivalent to what will be collected in the whole Phase 1 period. The most important areas of improvement for the pixel detector that have been identified are: increased radiation hardness of inner layers; improved rate capability; increased granularity, usage of smaller pixels without increasing the power budget per unit area.

A new pixel front end chip must be developed both for the ATLAS and CMS detector upgrades in order to guarantee high performances at hit rates up to 2 GHz/cm^2 and working reliably for ten years in extremely harsh radiation environments with up to 10 MGy total dose and 10^{16} neutrons/cm^2 fluence. Data output bandwidth will be very high, due to the higher particle rate and the experiments request to run at a much higher trigger rate. Very low noise performance from the very front-end analog electronics chain is also a must, since all possible sensors types considered for HL-LHC have to feature high radiation hardness and are characterised by small signal compared to present pixel sensors at LHC: the new chip must run with a low threshold in order to be highly efficient. Figure1 shows the main requirements for the new chip for phase 2 upgrade, compared with previous generation pixel chips: the challenge in performance from previous pixel chip generations is quite evident.

The choice of IC technology is a delicate decision of utmost importance for such a long term and challenging project. Tolerance to the unprecedented radiation levels is one of the prime drivers,

PARAMETER or FEATURE	**1st generation LHC phase 0**	**2nd generation LHC Phase 1**	**3rd generation LHC Phase 2**
CMOS technology	250nm	250nm / 130nm	65nm
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~500 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	2 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 μm^2 50x400 μm^2	100x150 μm^2 50x250 μm^2	25x100 μm^2 50x50 μm^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	~1000 e$^-$
L1 Trigger Latency	2-3 μs	4-6 μs	10-20 μs
L1 Trigger Rates	100 KHz	~100 KHz	200-1000 kHz
ASIC side	~1 cm^2	~4 cm^2	1-4 cm^2
Hit memory per chip	0.1 Mb	1 Mb	~16 Mb
Chip output bandwidth	~40 Mb/s	~320 Mb/s	~3 Gb/s
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.6 W/cm^2

Figure 1: *Evolution of the main requirements of pixel chips for the innermost detectors at LHC among different generations.*

but the technology must meet several other specific requirements: appropriate for highly integrated analog/digital mixed signal designs; sufficient circuit density for both analog and digital functions; low power consumption; well defined and reliable design kit for complex modern technology; flexible access by the HEP community; affordable for small prototype circuits and for the very large final pixel chips, and finally long term availability from multiple vendors, as qualification, design, prototyping, testing and final production will stretch over a relatively long period of five/ten years.

The CMOS 130 nm technology is currently used for several short/mid term pixel projects in the HEP community (ATLAS IBL, Timepix, LHCb VELOpix, etc.), and has been considered as a possible option for the high luminosity CMS pixel upgrade. The development of a new generation pixel chip requires a real R&D effort using a higher integration scale VLSI technology. Already during the definition of the upgrade of Phase-1 pixel detector, the effort of setting up the development of a new generation pixel detector was started[5]. It is however estimated that CMOS 130nm technology does not offer sufficient logic density to fulfil all the requirements for a HL-LHC pixel upgrade.

With respect to the CMOS 130nm node, the 65nm technology node allows more compact digital logic and memories ($\times$4), higher speed ($\times$2), lower digital power per single circuit ($\times$4) despite being a mature technology and a stable technology node, being used extensively for industrial and automotive applications that require availability over extended periods. CERN, thanks to the micro-electronics department PH-ESE-ME, has recently finalised a market survey and tender to get appropriate access to a 65 nm CMOS technology from one of the largest IC foundry in the world. IMEC, a well-known European IC research institute, has partnered with this IC foundry to provide access for European universities and small business IC designers to fabrication facilities. At CERN the chosen 65nm technology has so far been extensively radiation tested up to a total dose of 3MGy with very promising results.

2. The RD53 Collaboration

A workshop[6] was held at CERN in November 2012 to collect the experience from experts in the field from CMS / ATLAS and other pixel projects/VLSI activities, interested to the development for HL-LHC: INFN was present with several experts. At the workshop CMOS 65nm technology seemed to be very promising for a new generation of pixel chips.

This workshop led to the constitution of the RD53 Collaboration with the proposal of a Research and Development (RD) programme for the development of pixel readout integrated circuits for extreme rates and radiation. The Institutes participating in the RD53 Collaboration proposed to pursue a coordinated effort of research and development as described in the Letter of Intent CERN-LHCC-2013-008 (LHCC-P-006)[7]. The proposal was presented to the LHC Committee on June 12^{th} 2013 and received the recommendation to create an RD group. The CERN Research Board approved the RD53 Collaboration at its 205^{th} meeting on August 28^{th} 2013. In order to be effective, RD53 is specifically focused on the design of pixel readout chips, and not on more general chip design or on other aspects of pixel technology. Although data rates, radiation levels, and trigger requirements are different, there is synergy with the development of pixel detectors for future e^+e^- linear collider detectors and therefore collaboration is foreseen.

RD53 Collaboration is now a recognised experiment with 20 institutes from nine different countries (Czech Republic, France, Germany, Italy, Netherland, Spain, Switzerland, UK, USA) and about 120 member with a large presence of chip designers. The collaboration has the support of both ATLAS and CMS and is almost equally composed by people from the two experiments. By internal constitution, a Memorandum of Understanding signed by all institutes, there are two co-spokespersons, one member of ATLAS and the other of CMS, a Collaboration and a Management Boards. There are six working groups: radiation qualification, top level design, simulation test bench, I/O, analog design, IP-block.

For the Phase 2 pixel projects, the inner pixel layer will be exposed to a Total Ionising Dose (TID) up to 10 MGy. Therefore RD53 has extended the characterisation up to these very high levels. There are clear indications that small size P-MOS transistors experience more significant degradation than N-MOS above the 5MGy level, but running at low temperatures and later annealing at higher temperatures seems to give very beneficial effects, leaving room for long term survivability of this technology in a pixel detector at HL-LHC. Significant additional work is required to develop an understanding of such effects. Different types of irradiation have started to be used (10 keV X-ray, low momentum proton, 1 MeV γ rays).

Very low power and very small area circuit implementations for the required digital logic per pixel cell and per pixel region (e.g. 4x4 pixel cells) will be explored, developed, simulated and implemented in a 65nm CMOS technology prototype chip. Different approaches to achieve radiation tolerance to the 10MGy level and SEU immunity in critical functions will be evaluated. Alternative logic architectures (gated clock synchronous, asynchronous, dynamic logic, etc.) will be evaluated and compared and the most efficient will be implemented in a pixel array chip

To handle such high data rates the hit information can be stored locally within the array as shown in Figure 2. Storing information from multiple hits from the same cluster together translates into significant savings in required storage resources. Sharing of latency buffers in particular leads to compact circuitry and low power. The exact way in which the hit data are stored must be opti-

mized for the new requirements and technology. What this means in practice is understanding how many pixels share storage logic (so-called regions), in what pattern, with what internal organization, and how are region boundaries handled. The optimisation of the region size does depend on cluster size distributions, which in turn depend on sensor type and location in the detector, and on physics input. It is also necessary to consider the grouping of the sensitive analog circuits into well-isolated analog islands, which will depend on the process options and on how power is distributed within the chip.

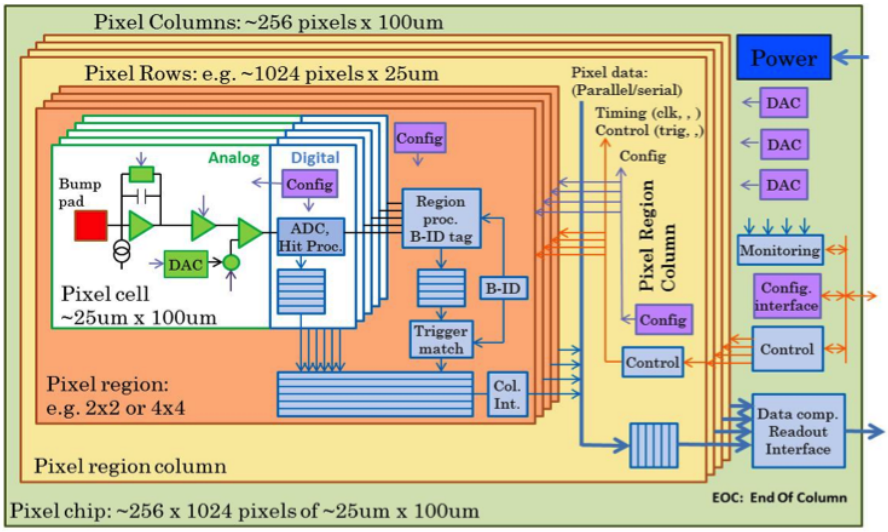

Figure 2: *Diagram of pixel hierarchical organisation and architecture*

In the RD53 time scale it is not foreseen to develop a common ATLAS and CMS pixel readout chip, but to boost most of the development, test and qualification effort needed that is independent of the specific implementation of the final chips for the two experiments. Multiple implementations are possible using the same technology foundation. In the timeline of the collaboration it is foreseen an RD53 prototype for the years 2016-2017.

3. The CHIPIX65 / INFN project

The HEP community has little or no experience with the use of CMOS 65nm technology for front-end electronics, while has already started its use in the back-end with the FTK project. INFN feels it is of outmost importance to have a leading role in the use of this new technology, that will open up new possibilities with implementation of local intelligence in the front-end, with low noise performance, and all this will make it possible to reach unprecedented performance in several detection systems.

For this reason seven INFN groups (Bari, Milano, Padova, Pavia, Perugia, Pisa and Torino) already part of the funding institutes of RD53, proposed to INFN the funding of a project for the development of an innovative CHIP for a PIXel detector, using CMOS 65nm technology. The CHIPIX65 project was approved by INFN National Scientific Committee 5 as Call project in October 2013, and counts 35 members experts on the field, of which 20 are actual IC designers,

constituting a substantial fraction of INFN expertise on microelectronics. The project is serving also the purpose of pushing the use of CMOS 65nm in the INFN across a wide community spread across several INFN groups.

The choice of a focused RD is to have a clear use-case and a clear deliverable with milestone and time schedule, discussed inside an international community of the LHC experiments. The interest of CHIPIX65 institutes to be in RD53, or to work together with it, is that it provides the collaboration framework to enable synergies at international level, sharing experience with world-wide HEP experts in the field and focusing on this common interest. It also allows to reach the best sub-division of work among participating members to guarantee the success of the defined RD project. CHIPIX65 is making the contribution of the INFN groups stronger and self-consistent inside such an international RD activity. This assures to maximise the overall results and experience obtained by the INFN institutes in the context of using modern radiation tolerant CMOS technologies for front end electronics and in particular for future generation pixel chips required for the HL-LHC.

CHIPIX65 project is contributing to most of the research lines needed for the new pixel chip. For the study of the radiation qualification of the technology, the involvement of Padova group is fundamental for the study of Total Dose (TID), Total Displacement Damage (TDD), Single Event Effects using respectively X-ray, low energy protons and heavy ions coming from, in order, the X-ray machine at Padova INFN, the Legnaro INFN facilities of SIRAD at the Tandem and the CN accelerator. The analog very front-end chain (preamplifier, discriminator, signal processing) is developed by the Torino, Bergamo and Pavia groups that are studying different architectures for synchronous and asynchronous front-ends, with very fast peaking time and low noise solutions, and are foreseeing different Time-over-Threshold measurement methods. The design of several IP-blocks are foreseen by RD53 and about one third of them are under the responsibility of CHIPIX65 like DAC and ADC (Bari), BandGap (Pavia, Bergamo), sLVDS-to-CMOS and CMOS-to-sLVDS transceivers (Pavia, Bergamo, Pisa, Torino), rad-hard by design memories like Dice SRAM[8] and logic (Milano), High Speed Serializer/Deserialiser (Pisa) and others like PLL are under discussion in within the RD53 and CHIPIX65. Under the study and definition of the digital architecture Perugia is mainly involved in using high-level modeling tools (SystemVerilog) in order to collect sufficient statistic on the actual performance of the system in very high rate, high energy physics experiments[9, 10]. The study of Input protocols to receive clock and trigger signals and commands to the chip is done by Pisa looking to data protection from SEU events using Hamming encoding or other options, while Bari is concerned in providing monitoring data from the chip.

In the year 2014, the CHIPIX65 project has designed the first CMOS 65nm design of prototypes for the first IP blocks and for the first small matrices of pixels dedicated to the study of analog very front-end architectures. The prototypes have been submitted as three different dices of 2x2 mm^2 to the foundry and are now under test in the different groups.

4. Conclusions

The impact of CMOS 65nm technology on the High Energy Physics Experiments will be very significant in the next years. The RD53 is a large international collaboration focused to exploit the novelty of the technology establishing the fundaments of a new generation pixel readout chip for

the HL-LHC experiments, planning a collaboration full size prototype before defining the final chip for the CMS and ATLAS experiments. The INFN has a strong interest in growing experience in CMOS 65nm technology for the use at HEP front-end electronics and has financed the CHIPIX65 project in order to boost this initiative. CHIPIX65 contributions to RD53 Collaboration are very substantial and have seen the first prototypes of important part of the chip already in the year 2014.

References

[1] T. Poikela et al VeloPix: the pixel ASIC for the LHCb upgrade 2015 JINST 10 C01057

[2] T. Poikela et al. *Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout* , 2014 JINST 9 C05013.

[3] G.Mazza, A.Rivetti et al *The ToPiX v4 prototype for the triggerless readout of the PANDA silicon pixel detector*, 2015 JINST 10 C01042

[4] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*, Nuclear Instruments and Methods in Physics Research Section A, Vol. 636, April 2011

[5] CMS Coll. *CMS Technical Design Report for the Pixel Detector Upgrade*, CERN-LHCC-2012-016 ; CMS-TDR-11. 2012

[6] ATLAS-CMS 65 nm pixel ASIC meeting, https://indico.cern.ch/conferenceDisplay.py?confId=208595 (2012)

[7] M. Garcia-Sciveres and J. Christainsen, RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation, CERN-LHCC-2013-008, http://cds.cern.ch/record/1553467/

[8] S.Shojaii, A.Stabile, V.Liberali *A Radiation Hardened static RAM for high energy physics experiments* Microelectronics Proceeding, MIEL 2014, 29^{th} International Conference on (doi: 10.1109/MIEL.2014.6842164)

[9] S.Marconi, E.Conti, P.Placidi, J.Christiansen, T.Hemperek *The RD53 collaboration's SystemVerilog-UVM simulation framework and its general applicability to design of advanced pixel readout chips* Journal of Instrumentation (JINST), JINST 9 P10005, (2014) (doi:10.1088/1748-0221/9/10/P10005).

[10] E.Conti, J.Christiansen, P.Placidi, S.Marconi *Pixel Chip Architecture Optimization Based on a Simplified Statistical and Analytical Model* Journal of Instrumentation (JINST), vol. 9, Issue 3, pp. 2 - 12, March 10, 2014. (ISSN: 1748-0221; doi: 10.1088/1748-0221/9/03/C03011)